Evaluation of Low-Cost ICT

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Abstract

In recent years Manufacturing Defect Analyzer (MDA) vendors have enhanced their offering to include power up options and limited powered test capabilities for digital devices. Since the capabilities have been increased one now has to think about the possibility of replacing traditional in-circuit testers. Throughout this paper an MDA system equipped with the enhanced options will be referred to as Low-Cost ICT (L.C. ICT).

The cost difference between the platforms can be as much as 6 times greater for a traditional ICT test station. The differentiator between the two platforms is that L.C. ICT only supports limited digital device testing. Although that traditional ICT is best equipped for digital device testing, a significant number of today's digital devices are not supported by the testers' standard model library, as well as the speeds that these devices run at. Many of the digital devices are rarely found to be "electrically defective". Consequently alternative test methods supported by both traditional and L.C. ICT have evolved that provide structural defect coverage for digital device I/O pins at a lesser cost.

Since many of the digital devices are not supported by the testers' standard library model database and alternative test methods exist that apply to both platforms, a case can be made toward the fact that the gap between these two platforms is quickly eroding.

Introduction

Traditional in-circuit test (ICT) systems gained wide acceptance as the choice front-end test method during the early 1980's.
Plated Through-Hole (PTH) technology was the norm and the Wave-Solder process was notorious for creating solder bridges between components' adjacent leads and production controls were limited on pick and place machines.
Unit Under Test (UUT) complete physical nodal access via a bed-of-nails fixture was guaranteed by the use of assigned test pads and or PTH components' protruding leads. With optimum UUT nodal access, most of the passive analog components could be tested for their values and tolerances. In the least a presence test could be applied that would detect that a component was placed in its assigned location and oriented correctly.
Large Scale Integration (LSI) devices were not yet prevalent and most of the digital devices populated on a UUT were testable using the test systems' digital I/O hardware resources along with its standard digital device model library.
Digital tests are intended to exercise a device I/O's as described by the manufacturer's datasheet however these tests are seldom accomplished at the actual microprocessor operating speeds.
Less than a decade later Surface Mount Technology (SMT) became common place in manufacturing. The defect spectrum shifted from solder bridges on PTH device leads to unsoldered pins on surface mount device (SMD) pins. The decreased use of PTH devices also led to a decrease in physical test access which

in turn equates to a loss of defect coverage at ICT.

The introduction of Application Specific Integrated Circuit (ASIC) and Digital Signal Processor (DSP's) devices also contributed to the lost of defect coverage. Many of these devices were not and still aren't supported by the test system digital model library.

Early attempts by test engineers at modeling unsupported devices with the intent of achieving defect detection resulted in limited coverage obtained after many long hours of coding and debugging.

Test engineers tasked with developing traditional ICT test-sets are faced with the fact that less of the available tester resources are being utilized.

Traditional versus Low Cost ICT

Low Cost ICT (L.C. ICT) as the name implies is associated with a lower cost of capital than traditional ICT. This is due to the fact that L.C. ICT systems only support limited digital resources. The intended use of the limited digital I/O resources included with the L.C. ICT system is not for allocating for digital in-circuit testing but rather for driving signals on nets that would otherwise inhibit a test from being applied. Examples of signals that would require constrain during testing are JTAG compliance enables, oscillator disables, chip enables, etc.

Additionally a L.C. ICT test-set development is more simplified and less costly than a traditional ICT test-set development since the digital devices are not modeled and debugged. Chart 1 delineates the test-set development cost difference between the two platforms.

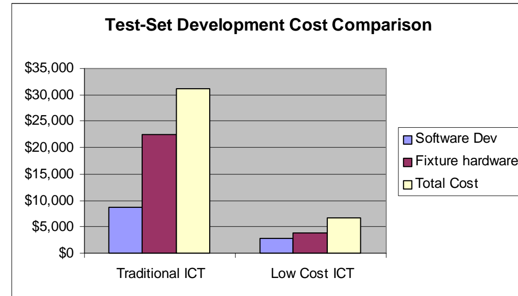

Chart 1

COMMON TESTS ENHANCING COVERAGE

Albeit that L.C. ICT only supports limited digital in-circuit testing, other test methods that are supported can detect most types of manufacturing defects. Table 1 itemizes the test methods supported and the potential defect detection achievable by each platform.

Test Method comparison

Test Method	Traditional ICT	Low Cost ICT	Defect Detection
Contact / Pins	Yes	Yes	BON probe contact to UUT, open traces to probed TP, missing / unsoldered components
Shorts /Opens	Yes	Yes	Undesired short / open nodes, presence of shunts and low value resistance
Analog (non-powered)	Yes	Yes	Incorrect passive component values (R,C,L), presnce (Q,D)
Analog (powered)	Yes	Yes	Incorrect frequency / voltage / current measurements,
Digital (non-powered vectorless)	Yes	Yes	Unsoldered digital device pins, rotated digital devices
Digital (powered)	Yes	*No	Model supported digital devices only (wrong / rotated / unsoldered / stuck at logic states), NAND / XOR Tree stuck at detection for compiant devices only, ISP / ISC for programmable devices. Must have physical access to most device pins
Boundary-scan	Yes	Yes	IEEE 1149.1 compiant devices only, wrong / missing / stuck at faults, OBP / ISC for programmable devices. Both support native and third part tools.

Table 1

Vector-less test methods such as Agilent TestJet and Connect Check [1] are not device model dependent and can be applied to most devices from the simplest to the most complex. Other test methods such as JTAG Boundary-Scan 1149.x [2], LSSD [3], NAND and XOR Tree tests are also available. These test

methods are supported by both L.C. and Traditional ICT platforms but can only be implemented successfully when compliant devices are populated on a UUT.

Although powered vectored digital in-circuit device tests can detect electrical device defects, not all electrical defects will be detected. These tests perform well when detecting stuck-at faults but will typically not detect at-speed faults such as transitional timing faults. Typically devices not supported by the testers' digital model library are tested by one of the alternative test methods previously mentioned.

A new concept in consideration is the integration of microprocessor specific JTAG In-Circuit Emulators (ICE) with an ICT fixture. This solution allows the ICT program to spawn to the ICE test suite and execute at-speed test routines. Basic microprocessor functions can be executed such as Start / Stop micro, Write to / Read from external memories and I/O ports, etc. This may sound unorthodox to some since the traditional ICT realm of testing and reporting faults one device at a time is contradicted. At-speed test routines may encompass numerous components when applied. An inconvenience noted with this method is poor fault resolution. When an at-speed test routine fails and indicts all components associated with the targeted cluster, it may take some time and effort to perform root cause analysis and identify the actual faulty component. Another ramification with this approach is that it is limited to products with on-board microprocessor that are supported by ICE hardware / software technology. The principle of testing component clusters at ICT is not a new concept however the use of an ICE to perform at-speed testing is innovative and leans towards the functional test domain. In the near future we may experience a trend at ICT where we see less digital in circuit testing and more at-speed functional testing.

Some will make a case against L.C. ICT systems having a greater potential of defect escapes than traditional ICT systems due to their limited digital test capabilities. Although there may be some validity in the above assumption, without quantifying the potential for digital device electrically defective escapes, the *risk* of not detecting these defect(s) during the L.C. ICT process will be unknown.

Additionally one must analyze whether specific defect(s) can ever occur and if they can, which test or inspection method would be the best candidate to detect the defect(s).

ICT Yield Details

ICT historical yield and defect details were solicited from multiple Jabil facilities. Chart 2 shows the percentages of confirmed electrically defective devices for each contributing facility as well as the overall average.

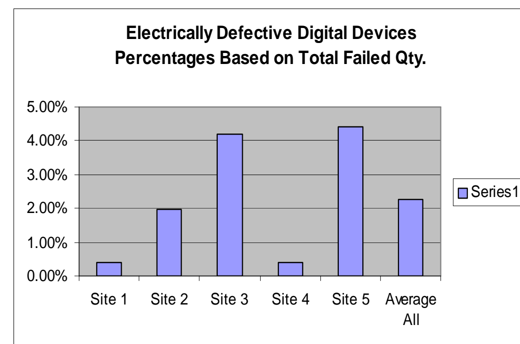

Chart 2

The data suggests that an average of 2.3% or less of the total tested digital devices is being confirmed as electrically defective at traditional ICT. In actuality, the accumulative average percentage stated may be even lower.

Opportunity exists for insufficiently soldered joints on SMT/SMD pins and BGA balls to manifest as an ICT digital device test failure. A Repair technician viewing an ICT failure report that indicts the device may not always locate the insufficiently soldered pin(s). The technician may choose to replace the device instead of re-soldering or re-flowing solder on the affected pin(s).

Future Work

Jabil has initiated a project in which both traditional and L.C. ICT systems will be placed side by side and a controlled-lot of product or test vehicles will be simultaneously tested on both platforms. Areas of interest will be categorized and weighted. Each vendor/test system will be scored based upon performance and cost as pertaining to each category.

- Total cost of ownership
  - Test System
  - Support / Training
  - Maintenance / Calibration / Repair
- Test-set development and debug times
- Test-set development costs
- Robustness of test fixture and test system fixture interface
- Accuracy of the measured data
- Repeatability of the measured data
- Percent of defect coverage achieved (Test-set effectiveness)

Categories pertaining to accrued time and cost can easily be measured and scored. The robustness of the test fixture will be measured against the Jabil Test Fixture Specifications [4] document. However until the developed test-set is fully debugged on the ICT station using a "Golden" board, the actual defect coverage achieved or the test-set effectiveness will be unknown. This is due to the fact that even though a test is generated for a particular component, the test once applied may not be able to properly detect a fault associated with the component. The generated test must be debugged and validated using fault insertion methods to determine its actual effectiveness. In order to fairly score "Percent of defect coverage achieved", a coverage analysis report will be documented for each vendor. The report will provide defect coverage details for all Nets and Device Pins. The report will be represented in the following format:

Net Name and Coverage Types:
NETS: Physical Access = Opens / Shorts test, Virtual Access Full = B-Scan interconnect test, Virtual Access Partial = B-Scan Chain Test Only, No Access = Not Tested
Device / Device.Pin , Coverage Type and Comment:
Vectorless: Testjet or IC Junction Diode
Analog: Presence Only, Presence and Orientation, Reel Value, Reel Value Kelvin, Characterized Value, Cluster, NO-POP Test, Not Tested
Powered Analog: Voltage / Current measurement, Frequency Measurement, Cluster Test, Hybrid Test
Digital In-Circuit: Presence, Presence and Orientation, Correct Device, OBP/ISP, NO-POP Test, "X"-Tree test, Cluster, Not Tested
Boundary-scan: Full (In-Out), Partial (In), None

Upon completion of the defect coverage analysis, an understanding of which devices will have defect coverage and which will not during the ICT test will be gained.

Summary

Increased digital device complexity and lack of physical UUT nodal test access has rendered traditional ICT expensive to implement on many products.

L. C. ICT systems support many of the same test methods used at traditional ICT with the exception of in-circuit digital device test resources. Many of the digital devices commonly used in products today are not supported by traditional ICT systems due to their increased timing set complexities.

Jabil historical repair data indicates that less than a 2.3% risk of “electrically defective” digital device escapes from ICT to FVT may exist for a given product.

Alternative test methods supported by both traditional and L.C. ICT platforms provide limited manufacturing defect coverage for most digital devices.

Innovative test techniques utilizing microprocessor based JTAG ICE are being explored that can provide at-speed test capabilities to ICT.

Jabil Circuit has initiated a project to evaluate low cost in-circuit test systems. Project details will be documented and presented at a later date.

Glossary:

ASIC: Application Specific Integrated Circuit
BGA: Ball Grid Array
BOM: Bill of Material
BON: Bed Of Nails
BSDL: Boundary Scan Descriptive Language
DFT: Design For Test
DSP: Digital Signal Processor
ICE: In Circuit Emulator
ICT: In Circuit Test
I/O: Input / Output
JTAG: Joint Test Action Group
LSI: Large Scale Integration
LSSD: Level-Sensitive Scan Design
MDA: Manufacturing Defect Analyzer
OBP: On Board Programming
PTH: Plated Through Hole
Reel Value: The component BOM value
SMD: Surface Mount Device
SMT: Surface Mount Technology
TAP: Test Access Port
UUT: Unit Under Test

Acknowledgements:

1) Jabil Advanced Manufacturing Technology Staff – St. Petersburg, Fl.
2) Jabil Test Engineering Departments – Globally

References:

[1] Agilent Technologies
[2] IEEE 1149.x Boundary-scan Guidelines
[3] IBM Corporation
[4] Jabil Global Fixture Specifications