Board Test Workshop 2005
Board Flex Initiative

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Agenda

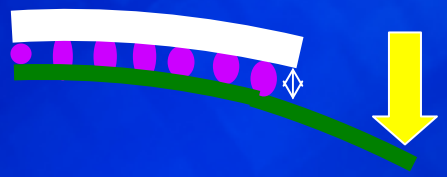
1. Introduction to Strain Measurement
2. Overview of Intel® Board Flex Initiative (BFI)
3. Test Equipment Requirements
4. Demonstration
5. Test Report Review
6. Jedec 9704
7. Questions and Answers

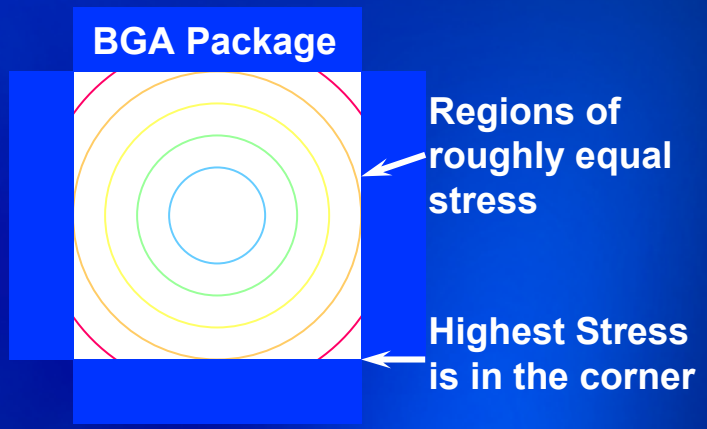
Intro to Strain testing

- As BGA package size and ball pitch have decreased, second-level interconnect failure due to manufacturing over-flexure has become an increasing concern, especially when combined with the metallurgical changes for lead free manufacturing.
- Data suggests typical manufacturing processes may exceed strain limits in one or more of these areas: Board Assembly, ICT, Functional Test and System Assembly
- In Circuit Testing (ICT) has shown to induce the highest strain.
- Strain gage measurement is a common and effective way of monitoring board flexure, and Intel® is now establishing strain limits for our BGA products.
- Intel's® BFI (Board Flex Initiative) is a set of tools that has been carefully designed to correlate laboratory experimental data to the real world factory.

Definition of Board Flexure

- When a board is assembled it is stressed—and therefore strained—in many directions. This "board flexure" puts stress on the solder joints and causes the package to flex, too. The corner solder balls are usually under the most stress.

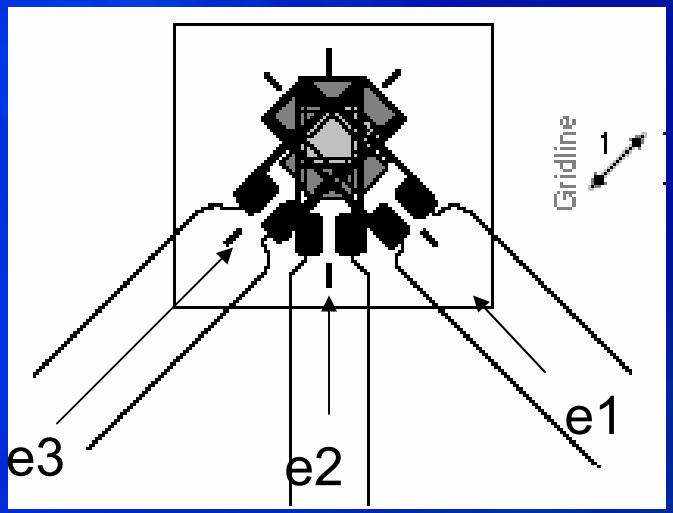




- We do not have a way to directly measure the stress or strain on the solder balls, so we measure the strain on the PCB near the corner of the package.

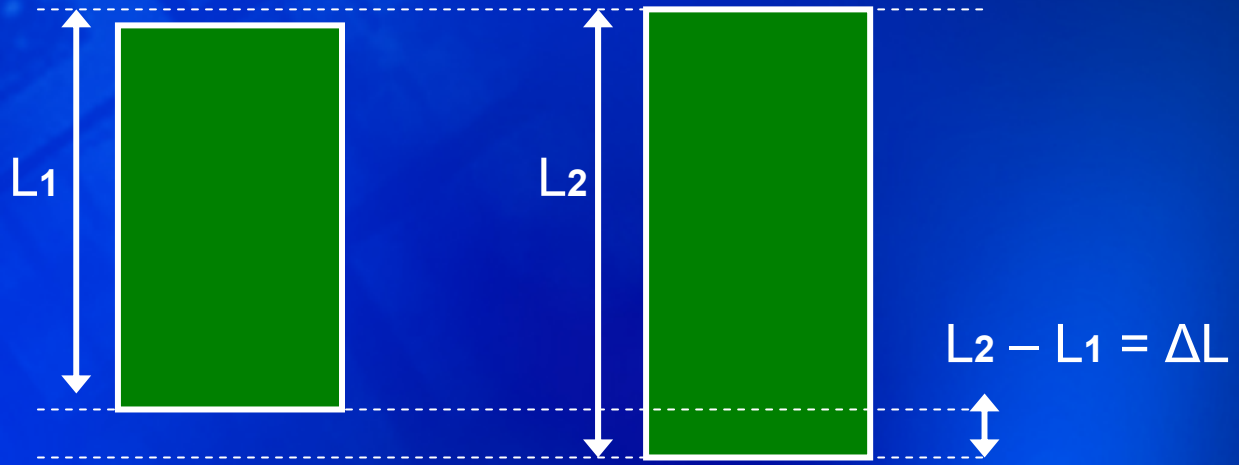
How do we measure strain?

- We measure strain using rectangular rosette strain gages that measure 3 directions at once. (e1,e2,e3)
- They work by measuring the resistance change that occurs when a metal is strained.



What is Strain?

- Strain is a measure of deformation, relative to the initial size.



- Strain is calculated using the formula $\varepsilon = \Delta L / L1^*$ which has no units since the lengths cancel out.
- When ε = 0.000001, it is called 1 microstrain (με).

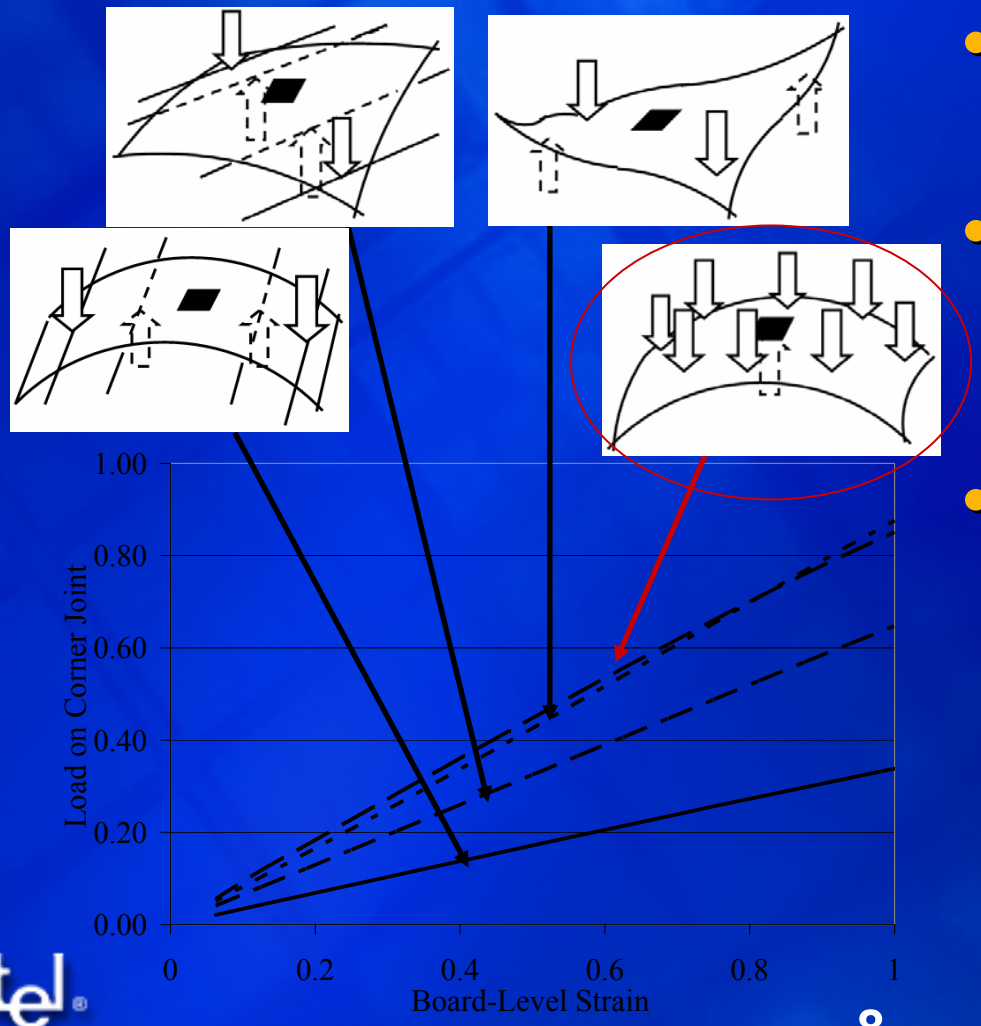
Strain Metrics

- Since Strain is a dimensionless number, a precise metric must be used to define the test values.
- The value is based on careful lab testing and analytical FEA methods.
- Intel® uses a metric called diagonal strain. This metric correlates better to solder joint damage, regardless of bend mode, than a many other metrics, including principal strain. The worst case bend mode for rectangular FCBGA components is Spherical bending.
- The diagonal strain equation is:

$$\text{Max Diagonal Strain} = \text{MAX}(|e2| , |e1+e3-e2|)^*$$

*Defined as the Maximum of the absolute value of either e3, or e1+e3-e2

A spherical bending condition is the worst case

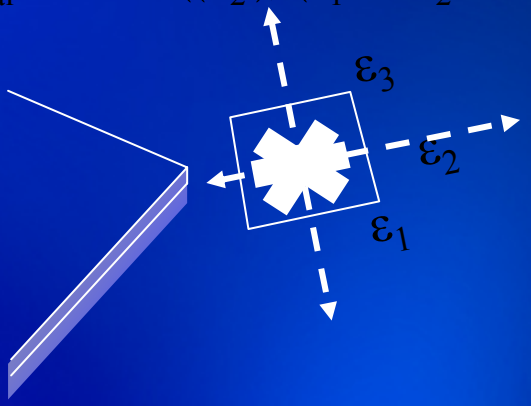


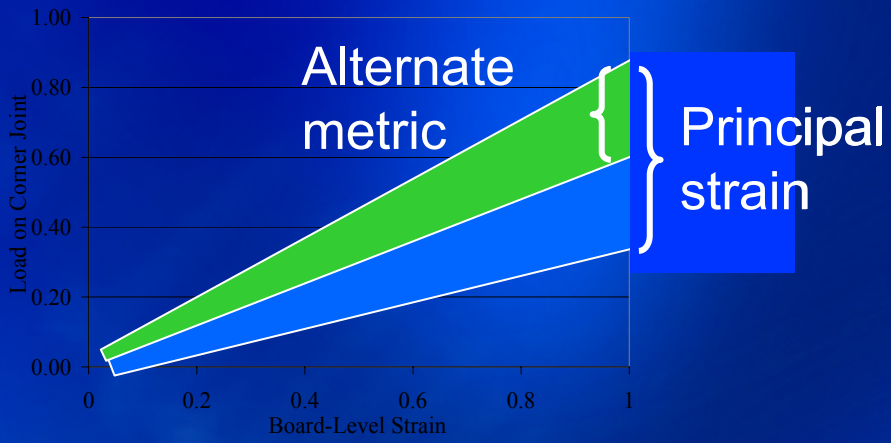
- Several bend modes were tested.
- Large variation was seen in the strain at failure
- Spherical bend gave the highest strain vs. joint stress

And is less bend mode sensitive

- This metric isolates the strain vectors most responsible for corner joint stress
- This results in reduced strain level variation at joint failure, regardless of bend mode, compared to principal strain

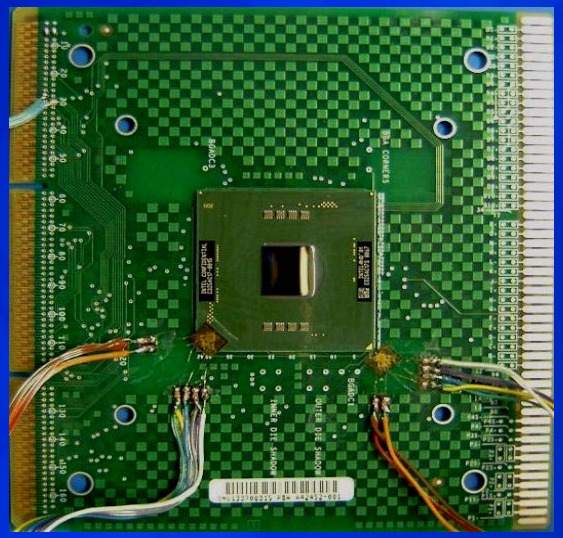
$$\varepsilon_{diagonal} = \max\left(\left(\varepsilon_2\right), \left(\varepsilon_1 \quad \varepsilon_2 + \varepsilon_3\right)\right)$$

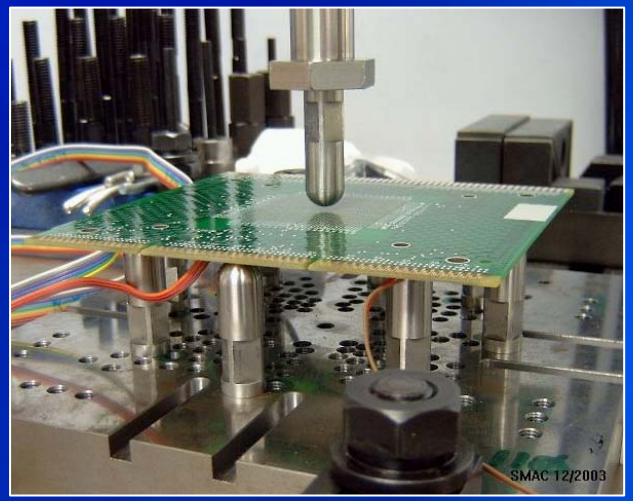




Strain Limit Determination

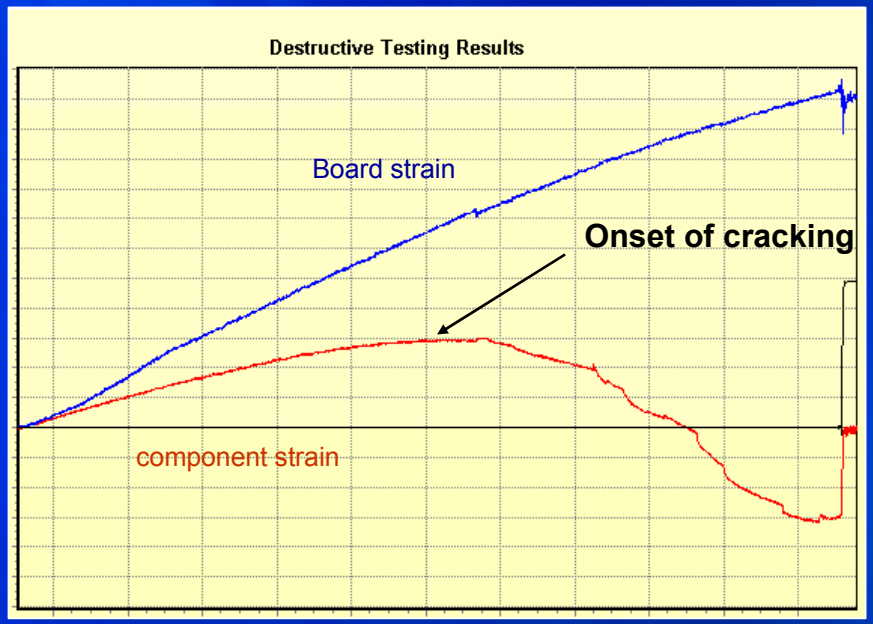
- Intel® has begun providing strain limits for its BGA components to help manufacturers identify processes which cause high strain.
- The limits are based upon a laboratory test in which pressure is applied to the back of the component and around the component in the opposite direction. We test for the strain at which cracks begin, not just when the electrical connection is broken.





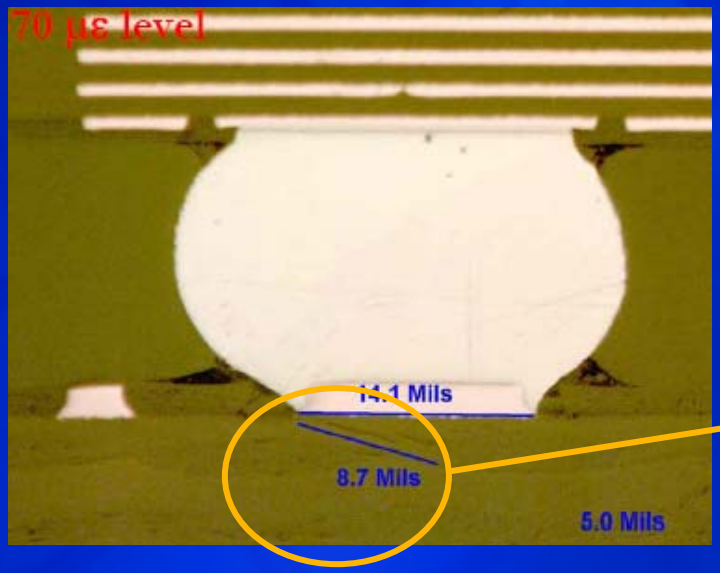
Strain Limit Determination

- Strain gages are attached to the test coupon at precise locations, the coupon is bent to certain strains, and the joints are tested for cracks.
- The result is a strain value for a particular location which is relative to the threshold of damage.



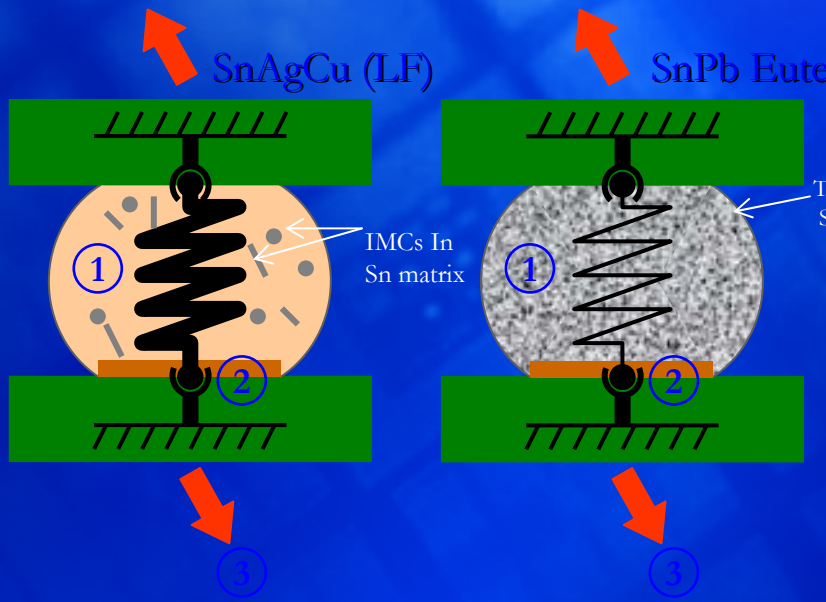
Strain Limit Definition

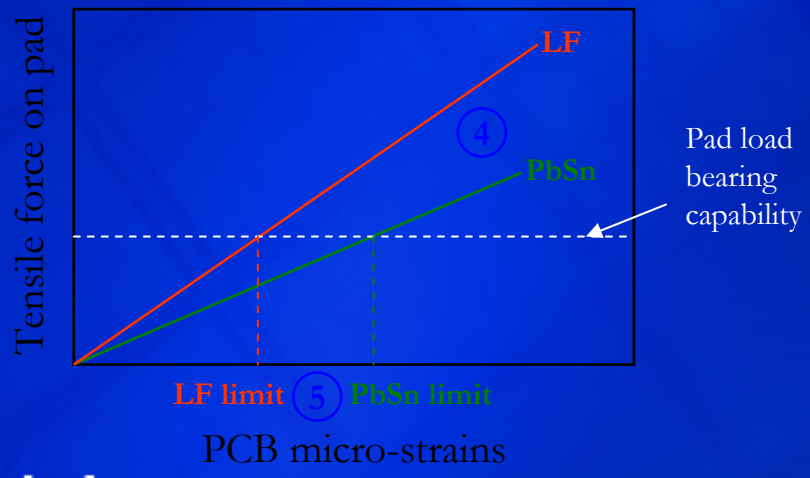
- The test is designed to define the degree of board flex at which point board crack initiation begins not when the an electrical open occurs.



Example of over-flexed condition. Note the board crack.

LF Solder vs Tin-Lead Eutectic Solder Comparison in Transient Bend

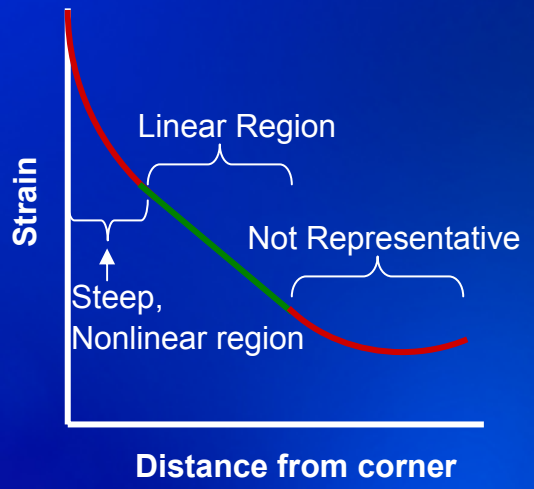




1. The solder ball joins the substrate and the PCB by material that behaves as a spring. Lead free solder has higher stiffness than PbSn solder, analogous to having a robust thick-wire spring coil for lead-free compared to a thin-wire spring for PbSn solder.
2. The bottom of the solder ball is attached to the PCB. The strength of the attach point is determined by pad size, PCB material and construction, etc. The interface strength (i.e. load bearing capability for pad crater mode) between the copper pad and PCB has not changed between PbSn and LF.
3. Board bending to a given micro-strain on the PCB is tantamount to pulling apart at an oblique angle the two opposite surfaces of the solder ball to a given amount.
4. The higher stiffness lead-free ball generates higher forces on the pad for the same applied deflection. The softer PbSn balls deforms more to accommodate the applied bending, resulting in lower forces acting on the pad for a given deflection level.
5. Since pad adhesion strength has not changed, lead-free ball reaches the critical level of force required to pull the pad out at lower strain. This is a consequence of the ball material property, not the pad property.

Precise gage location is critical

- Close to the joint the strain field is highly nonlinear
- Far from the joint the strain field is not representative
- For typical motherboard applications, 5mm from the package edge works well



Intel® Board Flex Initiative Overview

- The Intel® Board Flex Initiative (BFI) consists of six documents describing the theory and operation of board flex testing to reduce strain in the manufacturing environment.
  - Section 1 Introduction
  - Section 2 Gage Attach
  - Section 3 Calibration fixture
  - Section 4 Line testing
  - Section 5 Data Reduction
- These documents are available from TDE or your local Intel® test representative.

Desktop Components Strain Limit Guidance for Lead Free Package

Product	Package Pitch (mm)	Package Size (mm)	Board thickness (in / mm)	Pb-Free Strain Limit (με)
Intel® Broadwater GMCH FCBGA7	0.8+1.0	37.5 x 37.5	.040" / 1.0	600
			.062" / 1.6	600
Intel® ICH8 Chipset PBGA	1.07MM	31X31	.040" / 1.0	*500
			.062" / 1.6	*500
Intel® Gb-LAB "Ninevah" FCMMAP	1.0	10 x 10	.040" / 1.0	*500
			.062" / 1.6	*450
Intel® LGA775 Socket	1.27	45 x 45	.040" / 1.0	650
			.062" / 1.6	600

Important Note:

Above strain limit is only valid when using measurement metrology documented in Intel Board Flexure MAS rev 3.01 or later.

***Preliminary estimate**

Mobile Components Strain Limit Guidance for Lead Free Package

Product	Package Pitch (mm)	Package Size (mm)	Board thickness (in / mm)	Pb-Free Strain Limit (με)
Intel® Mobile 945 MCH Chipset	0.8+	37.5 x 37.5	.040" / 1.0	650
			.062" / 1.6	600
**Intel® ICH7M Chipset (Plastic Ball Grid Array)	1.07	31X31	.040" / 1.0	500
			.062" / 1.6	500
Intel® Pentium® M Processor in Micro-FCBGA Package (Yonah Based)	1.27	35 x 35	.040" / 1.0	*650
			.062" / 1.6	*650

Important Note: Above strain limit is only valid when using measurement metrology documented in Intel Board Flexure MAS rev 3.0 or later

*Assume Solder Mask Defined pads are used at corner.

**Not a FCBGA package, PBGA package.

Server Components Strain Limit Guidance for Lead Free Package

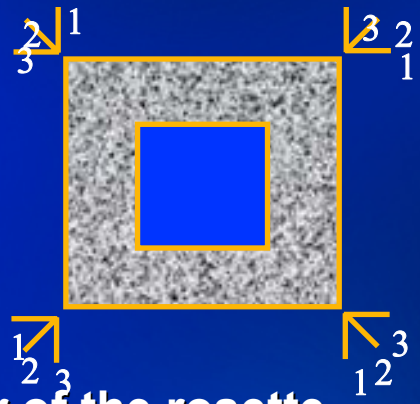
Product	Package Pitch (mm)	Package Size (mm)	Board thickness (in / mm)	Pb-Free Strain Limit (με)
Enterprise Southbridge ESB-2	1.0	40.0 x 40.0	.092” / 1.0	550
			.062” / 1.6	600
GMCH Northbridge Blackford/Greencreek	1.09	42.5X42.51	.092” / 1.0	550
			.062” / 1.6	600
Socket LGA771	1.27	45 x 45	.092” / 1.0	*600
			.062” / 1.6	*650

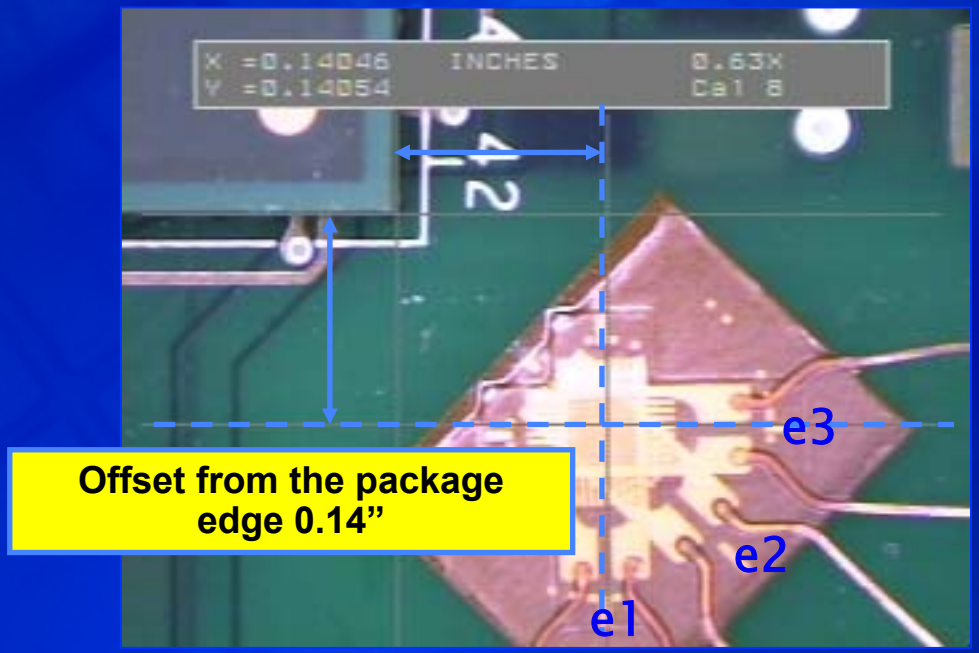
Test Equipment Requirements

- Data recorder parameters:
  - Minimum sample rate:
    - 500HZ for ICT
    - 200HZ for Functional Test
    - ½ rate if digital filter used.
  - Channel Sample Setup:
    - Minimum 3 channels
    - All Channels simultaneously
- The Data recorder must output the following 4 parameters for each gage:
  - Time (t), in seconds
  - Strain 1 (e1) in microstrain
  - Strain 2 (e2) in microstrain
  - Strain 3 (e3) in microstrain
  - The file can be a .TXT, or .XLS format.
  - 3 sample measurements run for each component

Gage Locations

- BGA rosette placement 4 gages
  - MCH, ICH, LAN or defined component

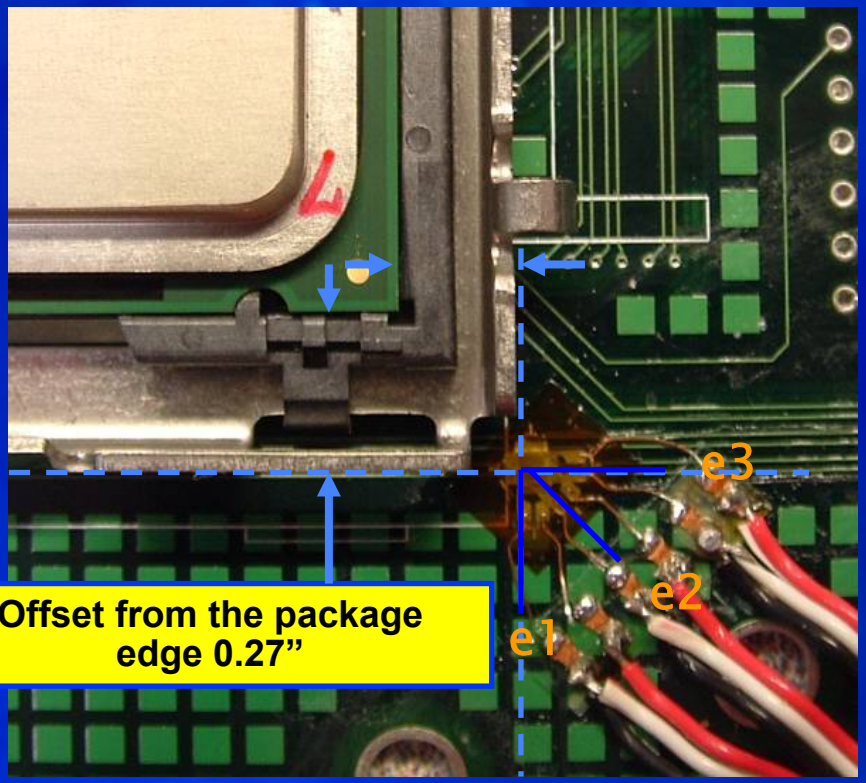


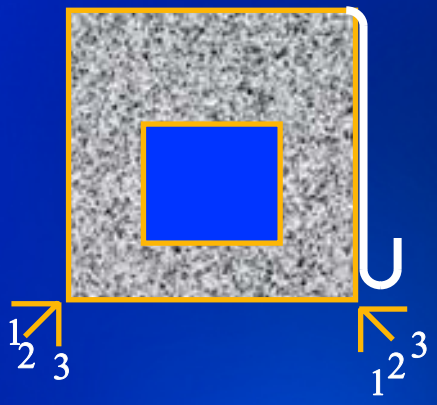


- The center of the rosette should be placed at the intersection of two lines offset from the package edge 0.14” +/- 0.01”
- Grid strains e1 and e3 should be oriented parallel to the edges of the package.
- e2 should be oriented diagonally away from package, with respect to the edges of the package, as shown.

Gage Locations

- LGA 775 socket- 2 gages only
  - rosette placement





- Attach rosettes at the two corners nearest the lever end.
- Place the rosette centers at the intersection of two lines offset from the component package edges .27” +/- .01”
- Orient rosettes as shown on the previous slide.

Data Report

- Data report is to be in one of the following Intel® Formats:
  - MAS 3.01 Section 5
- Data required in report:
  - Component identification
  - Board Identification
  - Component location
  - Gage make and type
  - MAX value E1,E2,E3
  - MAX DIAGONAL STRAIN for each corner
  - Digital Photo of each gage location
  - Graph of strain measurement from data acquisition system. Should contain e1, e2, e3, and if possible e4.
  - Components measured-MCH, ICH, LGA775

Demonstration

- Flex test run #1
- Diagonal Strain data reduction
- Strain Graph creation
- Report

Sample Report

Information		Data Acquisition System	
Company	Intel	Machine Make / Model	Manufacturer of Data Acquisition Syste
Site	Oregon	Machine Software / Version	Name of Strain Measurement Software
Product Name	BTX	Sampling Rate / Filter	g Rate / Analog Filtering Frequency Hz
Customer	Intel	**Strain Gage**	
Manufacturing Line	Franks lab	Gage Part Number	W-160-12
Date of Report	21-Aug-05	Gage Vendor	VISAHY
Inspector	Frank Joyce	Gage Description	Rect Rossette

Maximum Component Strain

				Values at Maximum Diagonal Strain				
Assembly Step	Component - Solder type - Board Thickness	Segment / Rep.	Strain Gage	Grid 1 microstrain	Grid 2 microstrain	Grid 3 microstrain	Diagonal Strain microstrain	Intel Strain Limit microstrain
System Assembly	LGA775 - SnPb - 0.062" - 1.5mm		A	-1286	357	-921	-2564	750

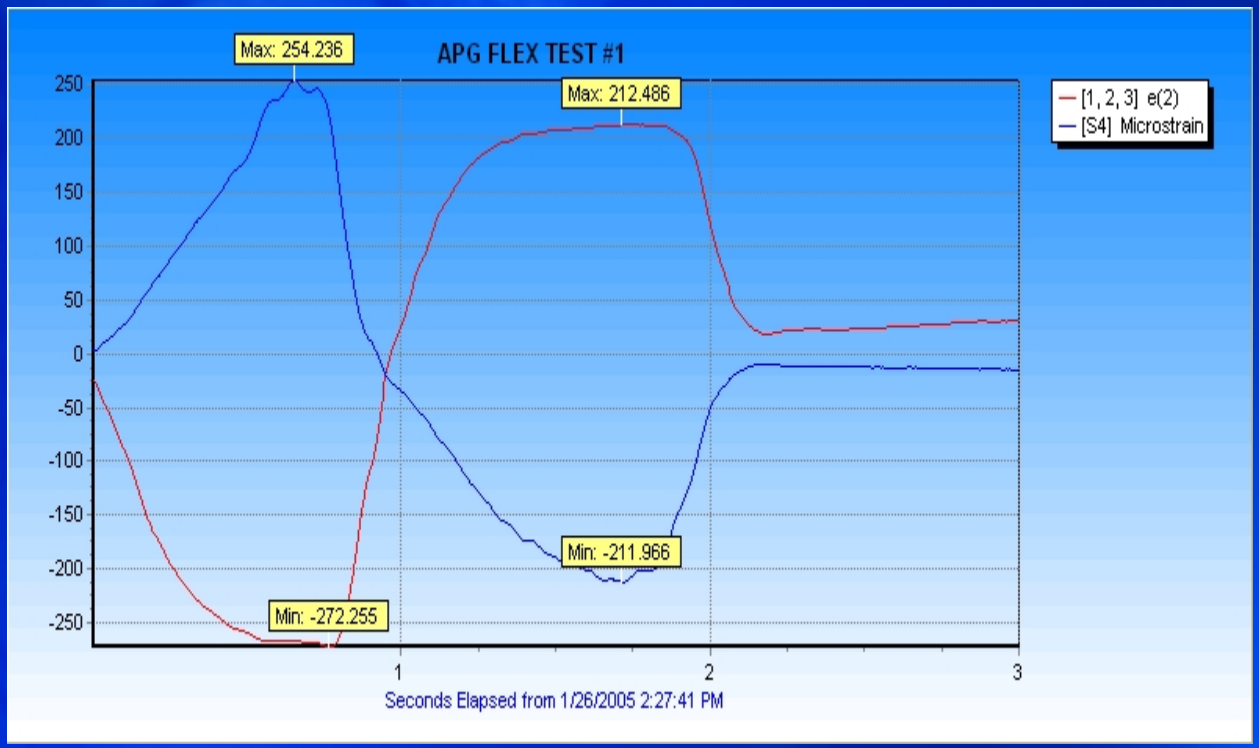
Summary of Strain Data

				Values at Maximum Diagonal Strain				
Assembly Step	Component - Solder type - Board Thickness	Segment / Rep.	Strain Gage	Grid 1 microstrain	Grid 2 microstrain	Grid 3 microstrain	Diagonal Strain microstrain	Intel Strain Limit microstrain
System Assembly	LGA775 - SnPb - 0.062" - 1.5mm		A	-1286	357	-921	-2564	750
			B	-983	-15	-541	-1509	
			C	0	0	0	0	
			D	0	0	0	0	
System Assembly	LGA775 - SnPb - 0.062" - 1.5mm		A	-1187	390	-986	-2563	750
			B	-932	-4	-574	-1502	
			C	0	0	0	0	
			D	0	0	0	0	

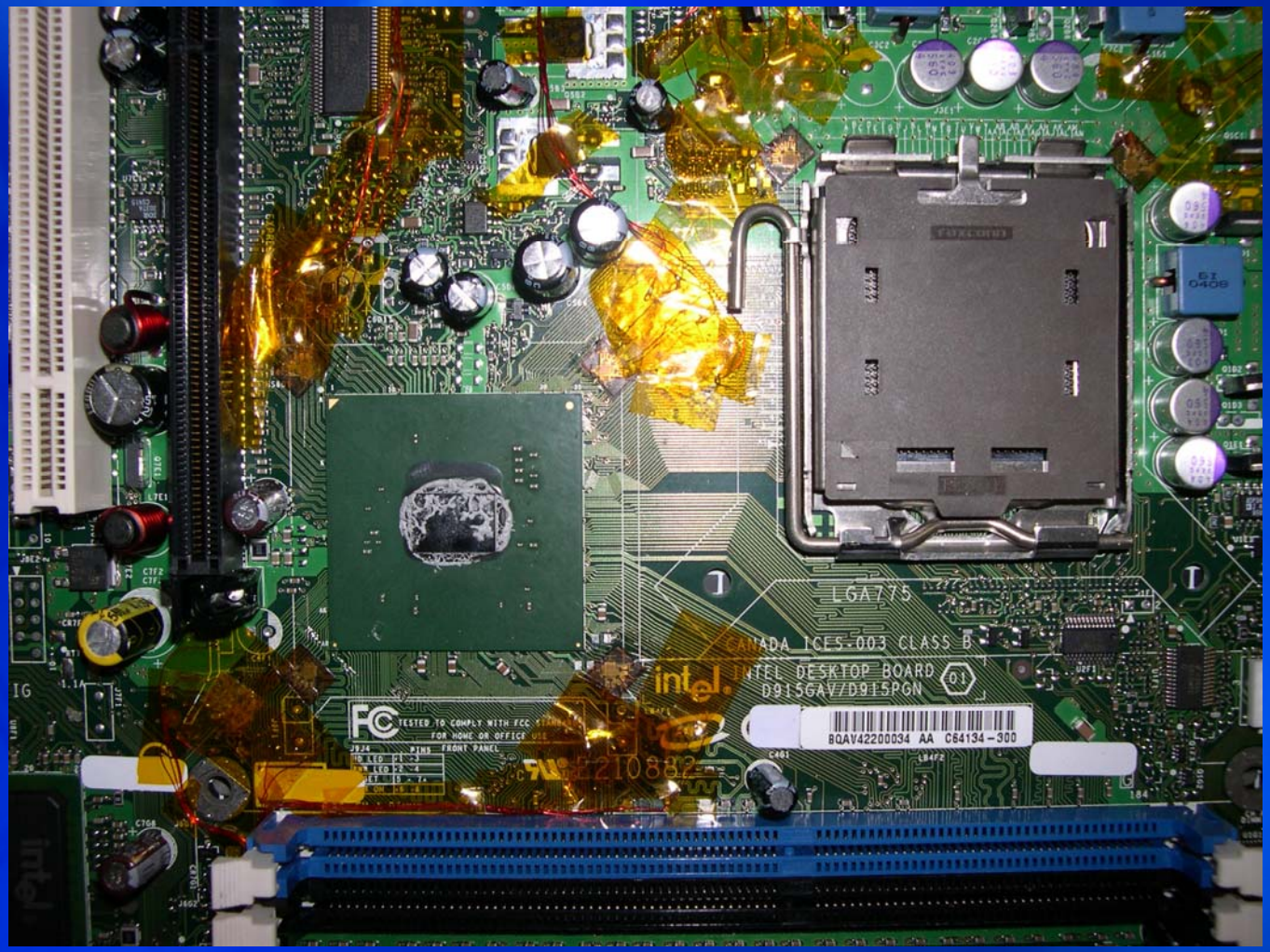
Sample Report

Sampling	Strain at Max Diagonal				Corner A		Strain at Max Diagonal				Corner B	
Rate	e1	e2	e3	ed	ep max	ep min	e1	e2	e3	ed	ep max	ep min
500	-1187	390	-986	-2563	402	-2566	-932	-4	-574	-1502	144	-1523
SecondsE	[1, 2, 3] e	[1, 2, 3] e	[1, 2, 3] e	ed	ep max	ep min	[4, 5, 6] e	[4, 5, 6] e	[4, 5, 6] e	ed	ep max	ep min
0.002	-1111	390	-1007	-2508	391	-2509	-938	-13	-570	-1495	10	-1518
0.004	-1112	390	-1007	-2509	391	-2510	-939	-14	-570	-1495	9	-1518
0.006	-1112	388	-1008	-2508	389	-2509	-940	-15	-571	-1496	8	-1519
0.008	-1110	389	-1007	-2506	390	-2507	-937	-13	-570	-1494	9	-1516
0.01	-1110	392	-1006	-2508	393	-2509	-936	-11	-569	-1494	11	-1516
0.012	-1108	393	-1006	-2507	394	-2508	-936	-11	-569	-1494	11	-1516
0.014	-1108	394	-1005	-2507	395	-2508	-935	-9	-569	-1495	13	-1517
0.016	-1111	394	-1006	-2511	395	-2512	-936	-11	-569	-1494	11	-1516
0.018	-1111	391	-1007	-2509	392	-2510	-938	-13	-570	-1495	10	-1518
0.02	-1112	390	-1007	-2509	391	-2510	-938	-13	-570	-1495	10	-1518
0.022	-1113	388	-1007	-2508	389	-2509	-940	-15	-571	-1496	8	-1519
0.024	-1111	389	-1007	-2507	390	-2508	-938	-14	-570	-1494	9	-1517
0.026	-1109	392	-1006	-2507	393	-2508	-936	-11	-569	-1494	11	-1516
0.028	-1109	392	-1006	-2507	393	-2508	-936	-11	-570	-1495	11	-1517
0.03	-1108	394	-1005	-2507	395	-2508	-935	-10	-569	-1494	12	-1516
0.032	-1110	395	-1005	-2510	396	-2511	-936	-10	-568	-1494	12	-1516
0.034	-1111	392	-1007	-2510	393	-2511	-938	-12	-570	-1496	10	-1518
0.036	-1112	390	-1007	-2509	391	-2510	-937	-13	-570	-1494	9	-1516
0.038	-1113	390	-1007	-2510	391	-2511	-939	-14	-570	-1495	9	-1518
0.04	-1111	388	-1008	-2507	389	-2508	-939	-15	-571	-1495	8	-1518
0.042	-1110	390	-1006	-2506	391	-2507	-937	-12	-570	-1495	10	-1517
0.044	-1109	393	-1006	-2508	394	-2509	-936	-11	-570	-1495	11	-1517
0.046	-1108	393	-1006	-2507	394	-2508	-935	-10	-569	-1494	12	-1516

Data Reduction Demo

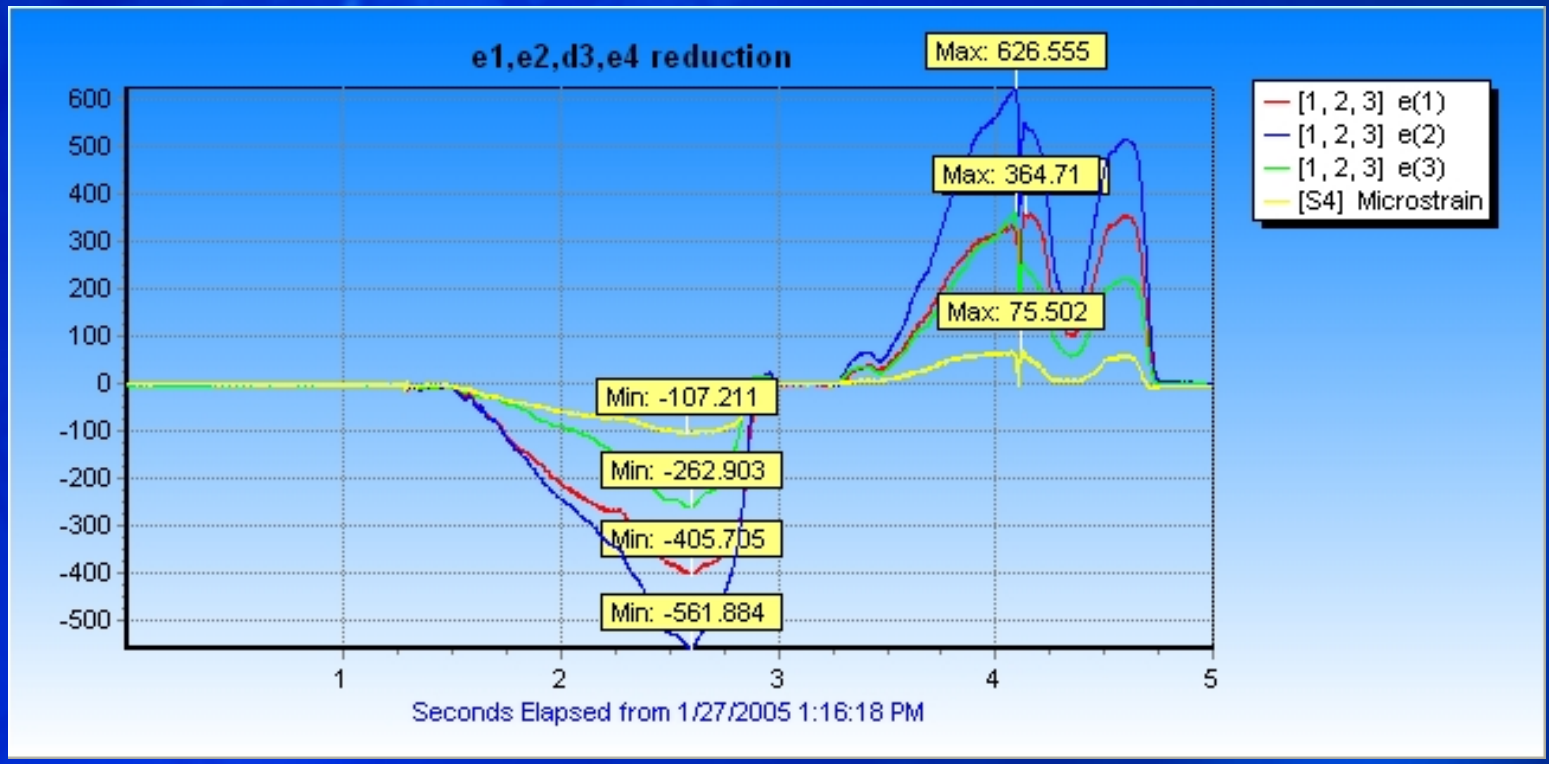


Gage Locations



Strain Graph

- Single corner 3 gage rectangular rosette data reduction graph



JEDEC 9704

- Jedec Spec

Future

- Alternate gage locations
  - Mobile and Handheld
- Tier 2 training videos
- Inclusion of 9-point bend into JEDEC

Backup