Trainer 1149:
A Boundary Scan Simulator
... and other aspects/examples of academic R&D in DFT

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Outline

- Short demo
- Comparison of similar tools
- Future work

- Are there any other training tools?
- Touch points between academia and industry
- Where is the academic research on board testing?
The system supports:

- Simulation of TAP Controller operation
- Illustration of work of BS registers
- Insertion and diagnosis of interconnect faults
- Different fault types are supported (shorts, opens, etc.)
- Test programming, executing, exporting (SVF)
- Work with training hardware
- Importing BS chips (BSDL)
- Design/description of the target board using several chips

... more ideas are still to come

http://www.pld.ttu.ee/applets/bs
Trainer 1149 demo

http://www.pld.ttu.ee/applets/bs
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JTAGer by FEUP (Portugal)
BScan Coach by Goepel

http://www.goepel.com
## Comparison to other similar tools

<table>
<thead>
<tr>
<th></th>
<th>Trainer 1149</th>
<th>Scan Educator</th>
<th>BScan Coach</th>
<th>JTAGer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Platform:</strong></td>
<td>Java</td>
<td>DOS</td>
<td>Windows</td>
<td>Windows</td>
</tr>
<tr>
<td><strong>Usage:</strong></td>
<td>web/local</td>
<td>local</td>
<td>local</td>
<td>local</td>
</tr>
<tr>
<td><strong>Chip editing/import:</strong></td>
<td>yes (BSDL)</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td><strong>Board editing:</strong></td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td><strong>Fault diagnosis:</strong></td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td><strong>Various fault models:</strong></td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td><strong>Test programming:</strong></td>
<td>yes (SVF)</td>
<td>no</td>
<td>no</td>
<td>yes/language</td>
</tr>
<tr>
<td><strong>Visualization:</strong></td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td><strong>Built-in help/tutorial:</strong></td>
<td>limited</td>
<td>splendid</td>
<td>nice/limited</td>
<td>no</td>
</tr>
<tr>
<td><strong>Built-in examples:</strong></td>
<td>unlimited</td>
<td>few/fixed</td>
<td>one/fixed</td>
<td>no</td>
</tr>
<tr>
<td><strong>Operates with HW:</strong></td>
<td>soon it will</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>
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Main future work directions

- Educational BScan hardware – first priority
- Logic cluster testing support
- Memory cluster test (P1581)
- 1149.4 and 1149.6
- Other new JTAG related standards/proposals (could be cJTAG, IJTAG)
- What else?
Discussion:

- Are there any other training tools?
- Touch points between academia and industry
- Where is the academic research on board testing?
Comments/questions by Ben and Bill

**Other training tools on DFT**

- What tools do you already have?
- How do you define the tools you create?
- How do the tools fit into the teaching process (e.g. used as demonstrators, hand-on laboratory sessions, etc)?
- What sort of reaction do you get from the students?
- How to obtain copies of the tools?
- Future plans for new tools.
- What extra help might you like, especially from industry?
Tools developed in TTU

**TurboTester** – a research environment with a large set of tools on digital test

**DefSim** - an integrated measurement environment for physical defect study in CMOS circuits.

**Web-based environment** for remote access to our tools

**Training software** on several topics of digital testing and DFT
Turbo Tester: an experimental research environment

Formats: EDIF AGM

Levels: Gate Macro RTL

Algorithms: Deterministic Random Genetic

Circuits: Combinational Sequential

Faulty Area

Specification

Design

Test Generators

BIST Emulator

Test Set

Fault Simulator

Multivalued Simulator

Fault Table

Logic Simulator

Defect Library

Hazard Analysis Data

Methods: BILBO CSTP Hybrid

Fault models: Stuck-at faults Physical defects

http://www.pld.ttu.ee/tt
http://www.pld.ttu.ee/webtt

September 15, 2006, Fort Collins, USA
Turbo Tester: an experimental research environment

Design Error Diagnosis

Test Generators

BIST
Emulator

Levels:
Gate
Macro
RTL

Fault Table
Test Set Optimizer

Methods:
BILBO
CSTP
Hybrid

Faulty Areas:
Combinational
Sequential

Logic Simulator

Formats:
EDIF
AGM

Defect Library

Hazard Analysis Data

Specification

Algorithms:
Deterministic
Random
Genetic

Multivalued

Fault models:
Stuck-at faults
Physical defects

Fault Simulator
DefSim IC details

- Standard industrial CMOS technology
- Area 19.90 mm²
- Approx. 48000 transistors
- 62 pins
- JLCC68 package

A built-in current monitor for $I_{DDQ}$ testing is implemented in each block.

http://www.defsim.com
DefSim Environment

Plug and Play – dedicated hardware and software

Experiment results 20:49:38, page 1
[ON1, single defect: n1/Q, Iddq activated]

DCBA  Q  PASS/FAIL
0000  1  PASS
0001  1  PASS
0010  1  PASS
0011  1  PASS
0100  0  FAIL
0101  0  PASS
0110  0  PASS

DefSim by TSTONICA

http://www.defsim.com
E-Learning software on DFT

Testing & Diagnostics

Basics of Test & Diagnostics

Applet supports action-based learning the basics of Digital Test. It offers a set of tools for understanding the principles of test generation, fault simulation, fault diagnosis and fault location in digital circuits. Built-in library of simple combinational circuits is given to train on the screen the main important techniques and algorithms.

RT-Level Test & BIST

Applet allows to solve and illustrate many RT-level problems of design and test of control intensive digital systems. Such topics as investigation of tradeoffs between speed and hardware cost in digital design, RT-level simulation, fault simulation, test generation, different techniques of built-in self-test (BIST) and other similar are covered by the applet.

Boundary Scan

Applet demonstrates principles of testing chips and boards, which have Boundary Scan structures inside. It simulates fault insertion and diagnosis, provides possibilities of combining own boards using built-in chip library or user imported chips.

Decomposition & Synthesis

Multiplicative Decomposition

Applet is devoted to general method of decomposition of FSM and enables synthesis of the network of interacting sub-FSMs corresponding to a complete set of partitions on the set of states of source FSM. We call this method of decomposition as multiplicative decomposition. 

http://www.pld.ttu.ee/applets
LFSR/BIST Simulator and Analyzer

Switching activity

Memory

Total Test Length (clock cycles)

Switches

0 20 40 60 80 100 120 140 160 180 200 220 240 260 280 300 320 340 360 380 400 420 440

0 500 1000 1500 2000 2500 3000 3500 4000 4500 5000 5500 6000 6500 7000

Select Estimation: c17 Estimation c3540 Estimation c432 Estimation
Select Real: c17 Real c3540 Real c432 Real

Clear table

Hybrid-BIST graphs

- Defect Loops
- Ignore Loops

Register Length

32 64 96 128 160 192 224 256

Operations

- Read vectors
- Attach Model

Status: Model: c132.asm

Number of clock cycles: 26

Characteristic Polynomial

Seed

001001100010010011010110110111001101

Set Reset Random

LFSR-Based Testing Principles Visualisation

Feedbacks

10111000101001110101001000101

Set Reset Random
Basic and advanced topics on testing

Logic level diagnostics

System level design and diagnostics

http://www.pld.ttu.ee/applets
Comments/questions by Ben and Bill

Academia and industry: touch points

- How does the work that you are doing act as a bridge between academics and industry?
- What kind of help can you use from the industry, and what can you offer to the industry as well?
- How much interest there is in board test in the academic level?
- Where is the greatest interest from the student level?
- What involvement do you have, or would like to have, with industry (in helping to define the tools before you build them, or playing with early versions to help debug, or donating expertise in running commercial tools, or allowing you to run their tools so that you can build up the experience, etc)
How does the work that you are doing act as a bridge between academics and industry?

- Helps educating (future) engineers/designers
- Promotes DFT ideas

- Currently on a small scale 😞

- Promoting our training tools and defining other necessary tools by industrial partners would help
What kind of help can you use from the industry, and what can you offer to the industry as well?

What we’d need:
- Close contacts to industry
- Formulation of real scientific challenges
- Commercial simulation/development environment

What we can offer
- Expertise in DFT
- Solving certain research problems
- Training
Where is the academic research on board testing?

- Liberec, Czech Republic - 1149.1, 1149.4
- Porto, Portugal - 1149.1, 1149.4, software
- Lubljana, Slovenia – BScan security issues
- Linkoping, Sweden - S-JTAG
- Jonkoping, Sweden - 1149.1, training board
- Oulu, Finland - 1149.4
- Tallinn, Estonia – 1149.1, training software
- Tokushima, Japan - current-based Board Test
Where are we?

- Estonia
- Finland
- Sweden
- Russia
- Tallinn
- Stockholm
- Helsinki
- St. Petersburg
Tallinn University of Technology

- Second biggest Estonian university with ~10 800 students. The **only technical university** in Estonia.
- Established in **1918** as engineering college, TTU acquired university status in 1936.
- A **three centered** university with 3 main cores – Technological, Natural and Social Sciences organized in 8 faculties.
- A **three-lingual** university (Estonian-Russian-English)
- A **campus university**.