Squeezing the power out of a Debug and Test Interface (DTI)

IEEE P1149.7, a complementary superset of the IEEE 1149.1 standard

P1149.7

An introduction to the proposed standard

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Presentation Outline

- P1149.7 history and status
- Why 1149.7?
- What can it do?
- What about performance?
- How does it work?
- How is it deployed?

1149.1 and P1149.7

What is their relationship?

- P1149.7 is ***not*** a replacement for 1149.1
- P1149.7 uses 1149.1 as its foundation
- P1149.7 provides 1149.1 extensions
- P1149.7 provides 2-pin operating modes

P1149.7 History and Status

- **MIPI Origins**
  - → Objective – define a backwards compatible minimum pin debug interface
  - → Strategy – requirements gathering, technical debate
  - → Tactics – solicit competing proposals, choose a winner
  - → Result – P1149.7 was handily selected as winning proposal vs. SWD

- **Collaboration with Nexus consortium**
  - → Objective – Compare common needs, explore common solution
  - → Strategy - Joint meetings, compare requirements
  - → Tactics - Specifications reviewed, incorporate feedback
  - → Result – Agreement to pursue IEEE standard because of large field of use

- **IEEE PAR approved**
  - → Test, Debug, and backwards IEEE 1149.1 compatibility considerations
  - → Specification reviewed and revision underway
  - → Presumed Result – IEEE 1149.7 standard in early 2007

Why P1149.7?

Harness 1149.1 entropy and provide a framework for creativity

- Addresses multiple on-chip TAP controllers
- Serves both applications debug and test needs
- More functions supporting applications debug
- Applications instrumentation over the same pins used for test

P1149.7 Activity

Engage Consortiums:

→ MIPI
→ Nexus
→ OCP

Engage Strategic Companies

→Silicon, Tools and Test:

- North America - Intel, Freescale, Xilinx, Corelis, EWA, etc.
- Europe - STM, Philips, Nokia, Lauterbach, etc.
- Asia - NEC, Fujitsu, Toshiba, Sophia, YDC, etc.

Engage “the Masses”

→IEEE 1149.7

Standards Focus

1149.1 vs. P1149.7

	1149.1	P1149.7
Test	Boundary Scan: Finding card level connectivity issues	Compliance: Preserving boundary scan for System on a Chip (SoC)
Apps		Capability: Features for debug

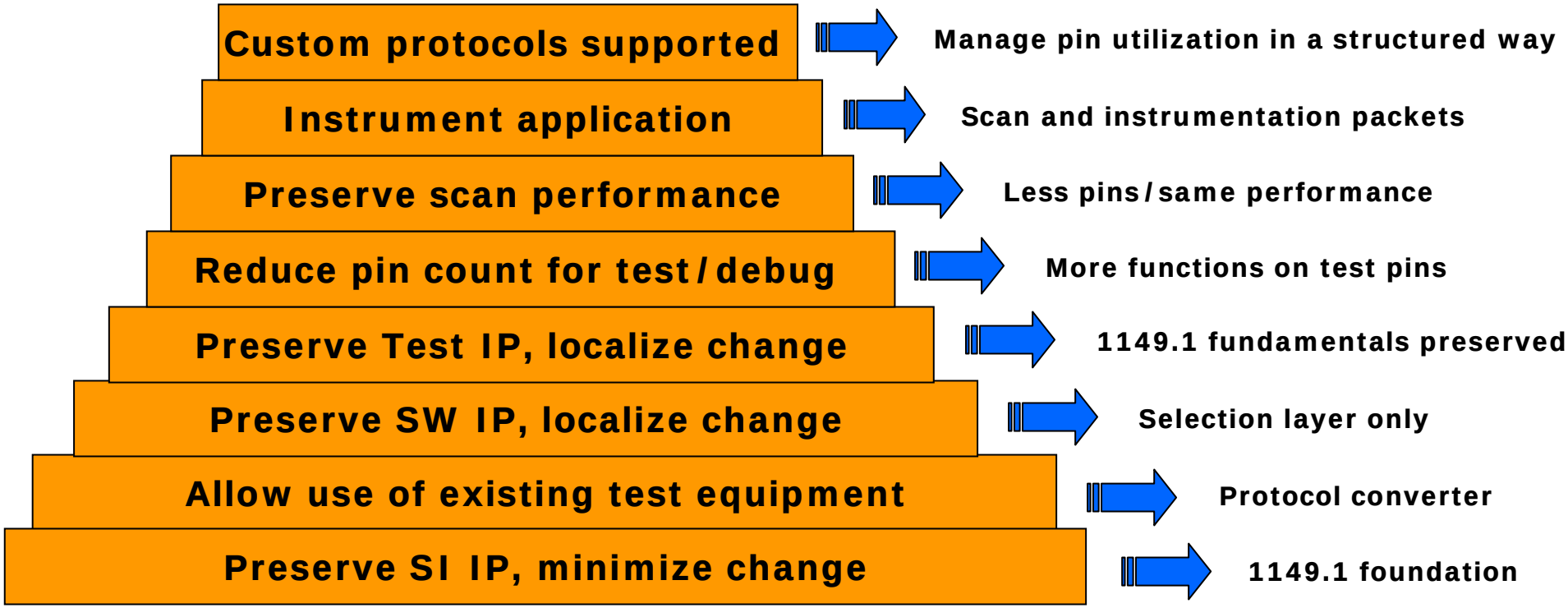
Key P1149.7 Objectives

- Do more with less
  - **Operate with fewer pins**
  - Add instrumentation using the same pins
  - TAP power management
  - Provide framework for diverse debug technologies
  - Preserve gateway to debug of SI errors/defects
- Preserve industry investment
  - SI IP
  - Software IP
  - Debug and Test Tools
- Provide means for innovation/customization
  - Pin protocols other than those supporting scan
  - Mix and match legacy/new IP
  - Equal treatment for all industry IP

Applications Debug Forces at Work

“Hold test gains while achieving better pin utilization”

Debug + Test >> ***“Make the right compromises”***



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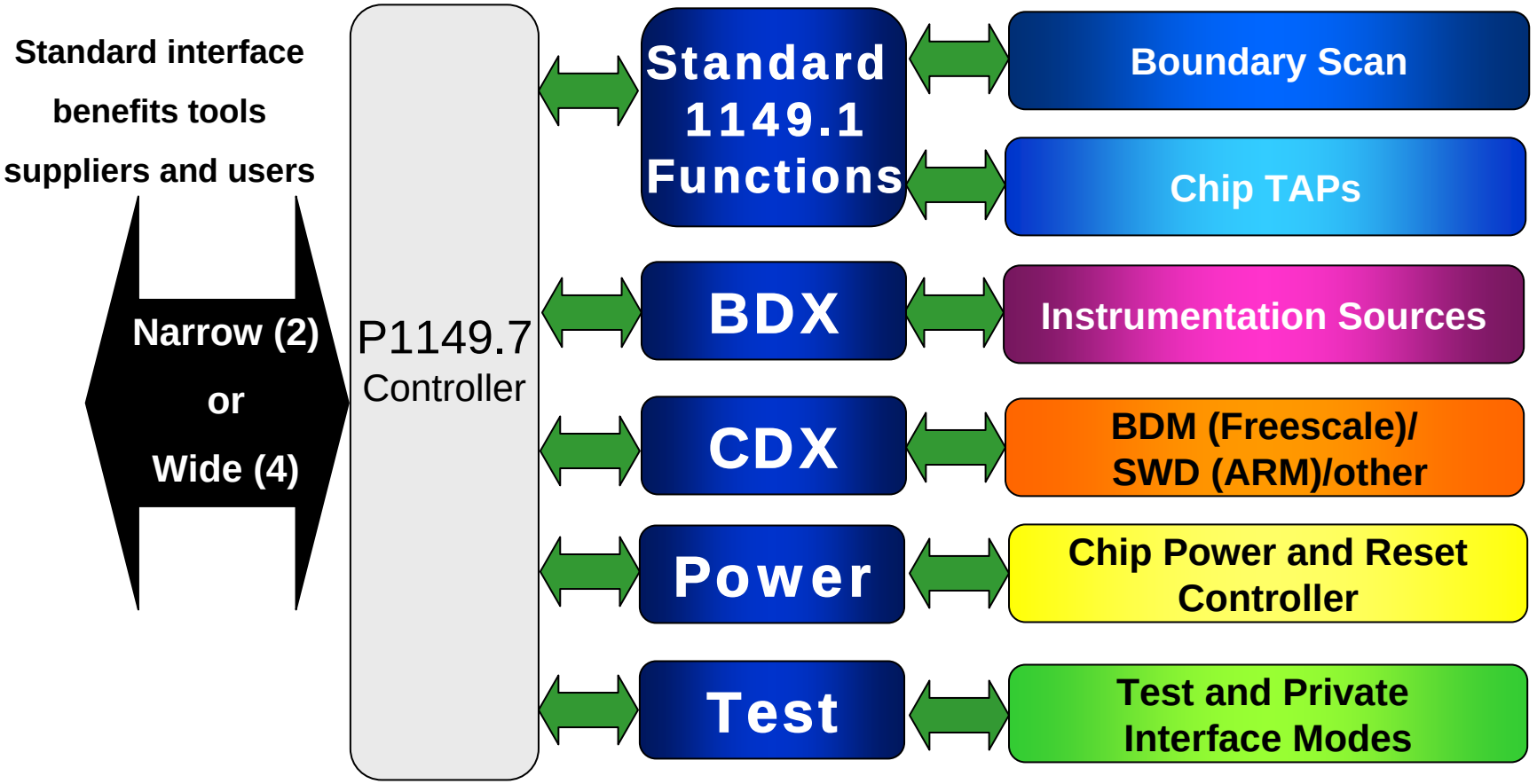
So, what can it do?

P1149.7 – A Debug and Test Tech. Binder

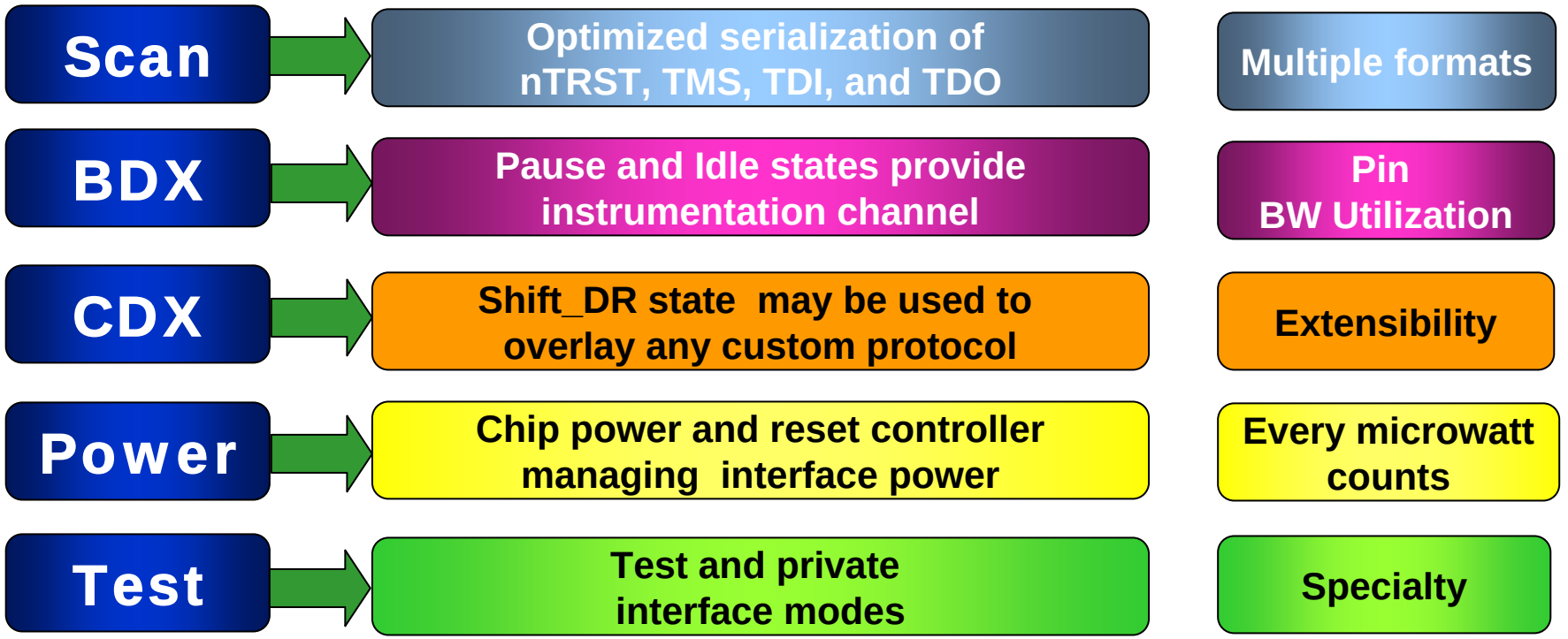
"All industry IP co-exists behind a standard Interface"



- Signaling is 1149.1 at start-up
- SW directed mode switches between use of standard and advanced protocol
- Once interface mode is set, software drivers communicate with standard 1149.1 protocol
- SW controls transmission efficiency by selection of transmission format best suiting system characteristics

A Look Inside P1149.7

"Major functions"



Deployment Profile

Minimal	Moderate	Most
Flash, CPLDs, FPGAs	SOC or Micro-Controller	Sophisticated SOC

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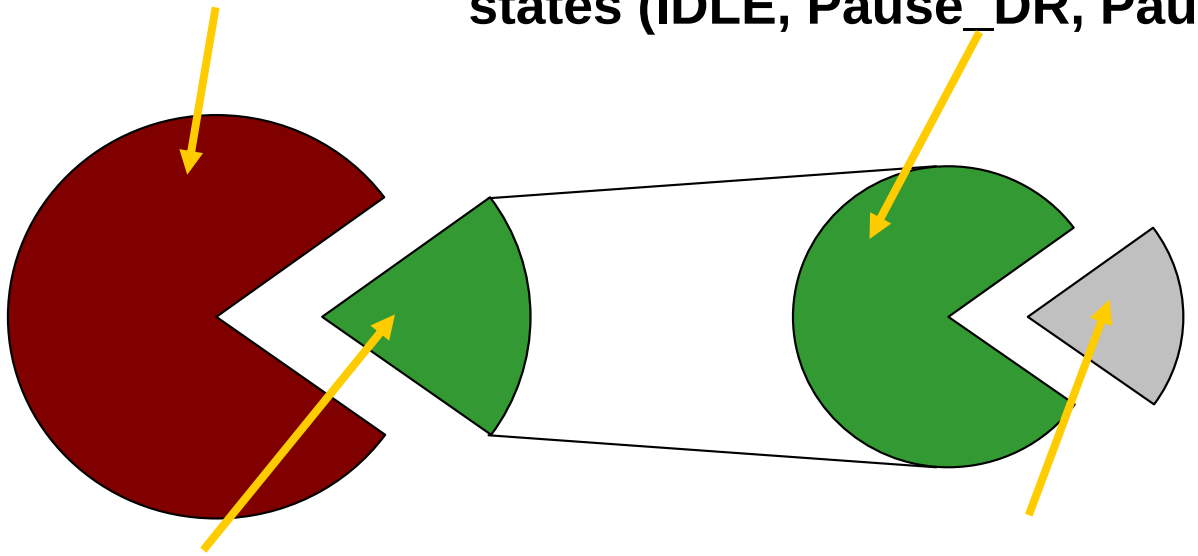
BDX – Better Use of Link BW

"The Compound 80/20 Rule of Interface Activity"

~80% of time is spent between actions

~80% of operating time spend doing an action is in parked states (IDLE, Pause_DR, Pause_IR)



~20% of time is spent using the link

~20% of operating time is spent doing useful work

Full link BW is needed for control ~ 4% of the time

Use Idle Control Periods for Background Data Exchange (BDX)

CDX – Custom Use of Link BW

“Supports vendor specific protocols”

- Redirects activity during Shift_DR states
- All controllers do not need to understand protocol
- Only device that is selected for scan participates
- DTS or Device may be master
- Different CDX formats may be TDMed
- Entirely under software control
- Can be invoked “inline” with scans

Full link BW is provide to any function

CDX follows BDX rules set only CDX manages line direction each bit

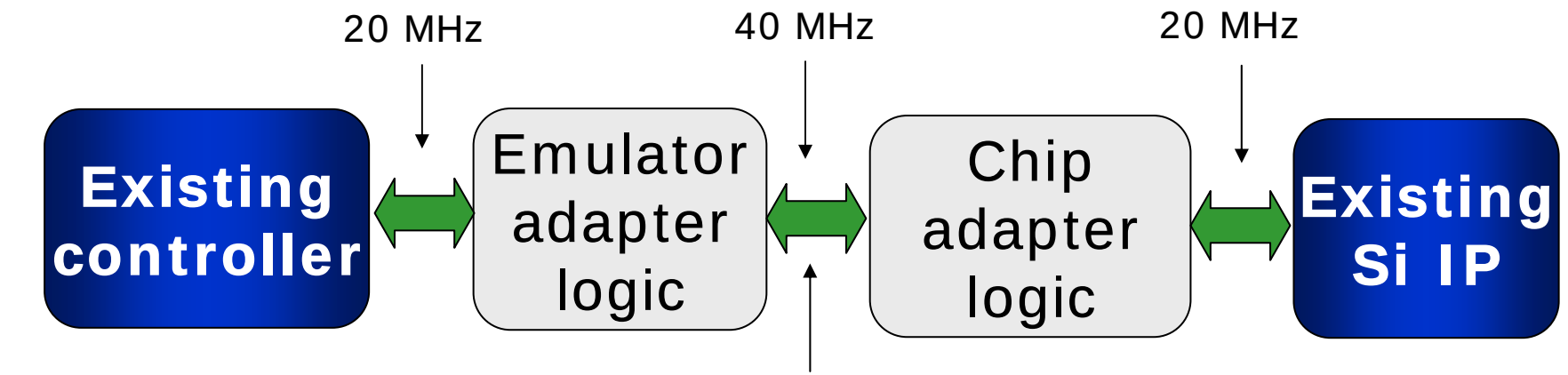
So, what about performance?

P1149.7 – Adds capability to 1149.1

"Minimizing Changes/Maintaining Performance"

- The same or better than IEEE1149.1 may be achieved in some cases
- With advanced protocol
  - Falling–edge to falling edge timing allows doubling TCK rate
  - The amount of information transferred is minimized to boost performance
  - Two or less bits are transferred/TAP controller state in some cases

2 bits/TAP state/ 2*TCK rate = the same TCK/TAP state rate as IEEE 1149.1



- P1149.7 added
- May be added to existing controller

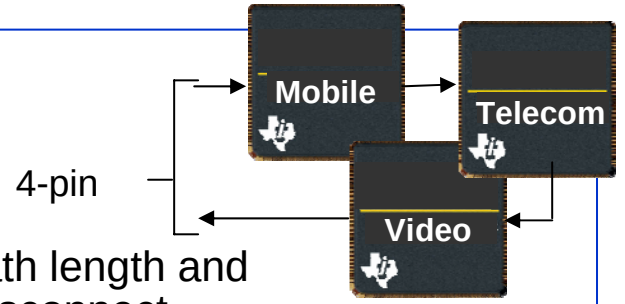
- P1149.7 added
- No changes to existing Si IP

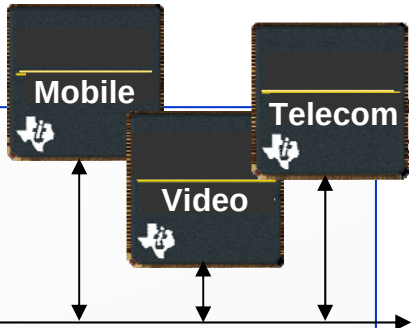
So, how does it work?

P1149.7 Overview

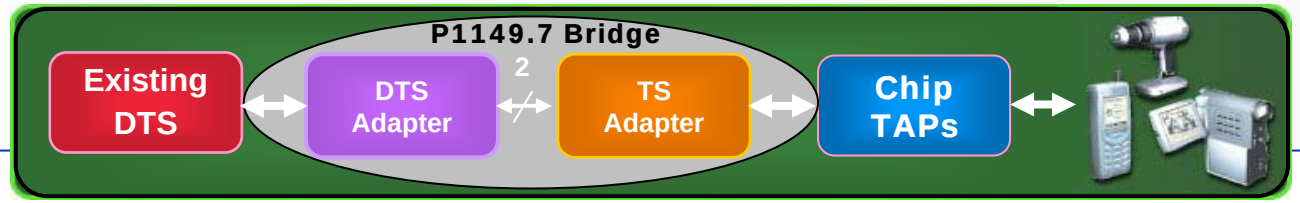
Extensions to the IEEE 1149.1 protocol

- Adds additional levels of control hierarchy
- Firewall and Super Bypass TM bit tackle series scan path length and system corruption with DTS and TS physical connect/disconnect



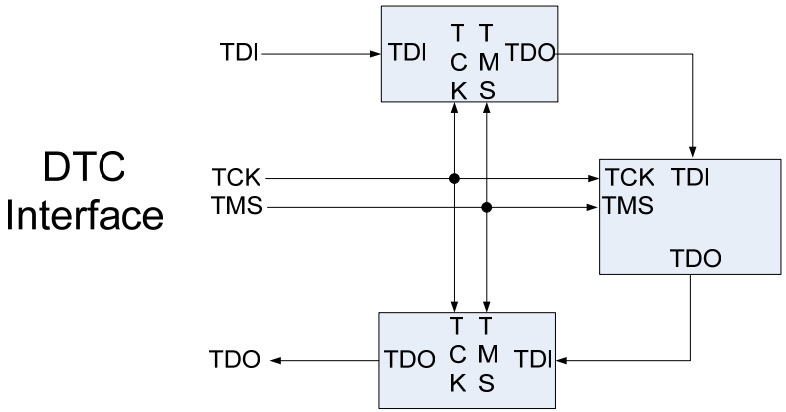


- **80 - 100 MHz operation**
- **1 or 2 Pins**
- **Combined scan/instrumentation/custom use of pins**
- **Glueless Interface to Multiple Devices (16 per DTS Port)**

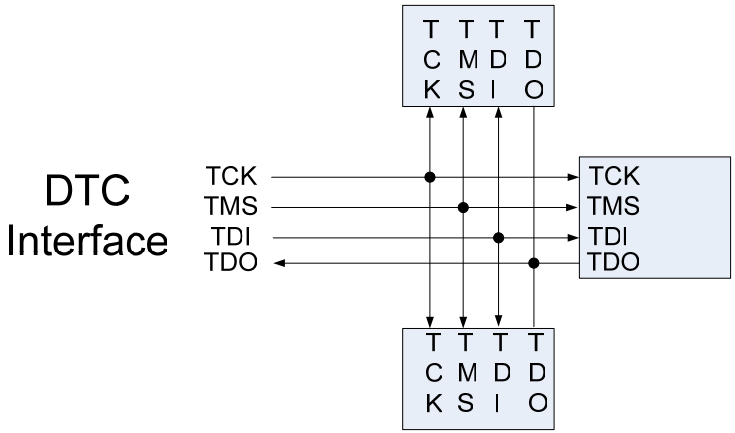


Connection Topologies

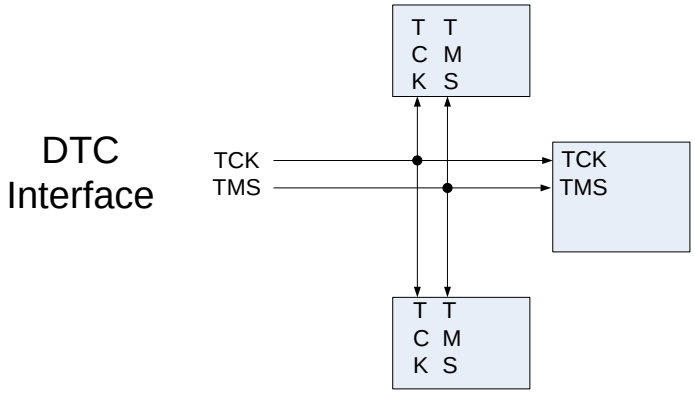
4-pin Series Scan Topology



4-pin Star Scan Topology



2-pin Star Scan Topology

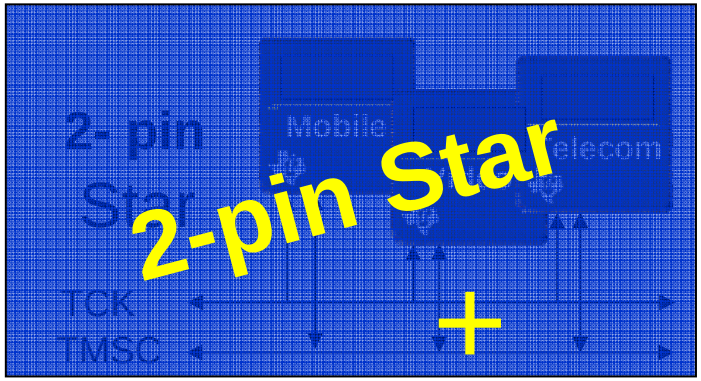


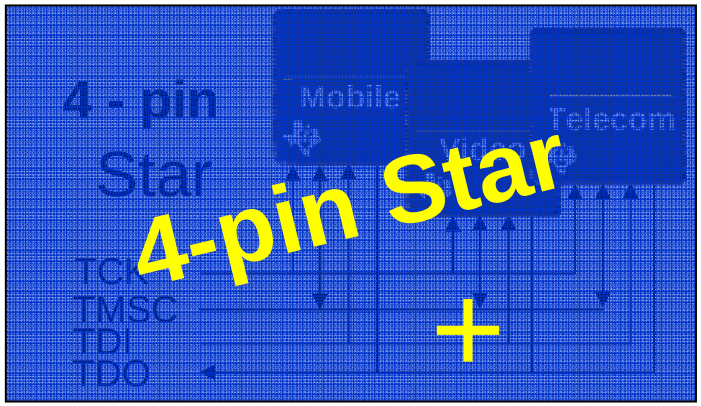
When all chips have Class 3 or Class 4 TAPs the 4-pin topologies may be operated as a 2-pin topology

Harmony with the 1149.1 Standard

SW IP Remains Virtually Untouched

(except for TAP selection layer)





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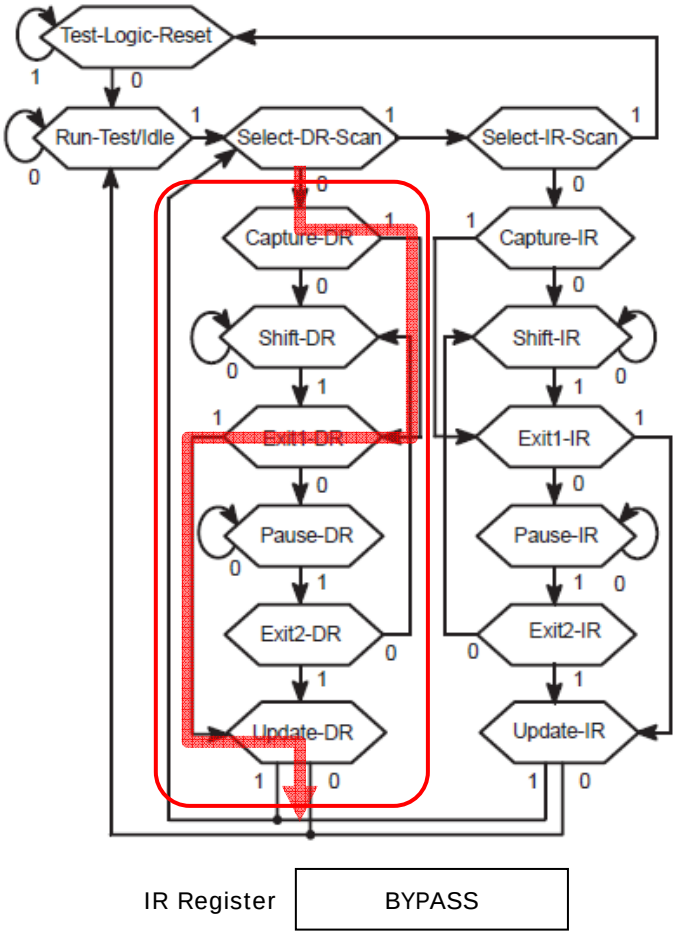
Key Control Concepts

- Extend functionality of BYPASS and IDCODE instructions
  ("overload" these instructions)
- Keep new command structure invisible to existing 1149.1 TAPs
- Create commands without using TDI or TDO
- Use commands to create registers without changing IR/DR scan paths

Overloading the Bypass Instruction (using Zero-bit DR-Scans (ZBS))



Method:

- IR register set to BYPASS or IDCODE instruction by:
  - IR-Scan or
  - Test-Logic-Reset
- ZBS = Capture→Exit→Update
- The number of consecutive ZBSs are counted to create a control level that specifies the overloaded function
- This is performed by standard IEEE 1149.1 TAP controller state sequences

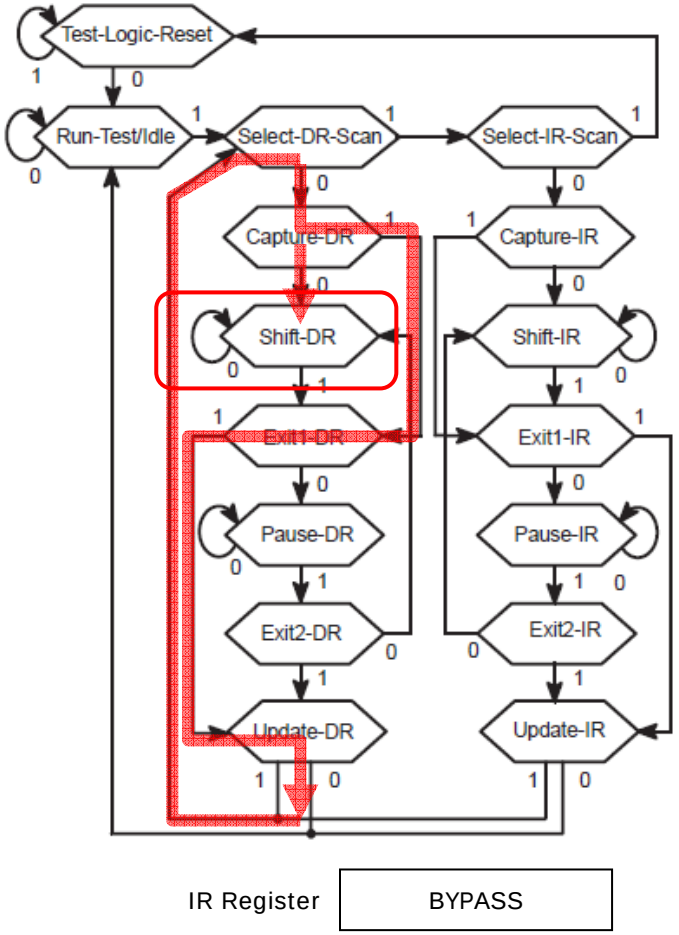
Zero-Bit Scans Create Control Levels

1….

2….

3….

Lock Control Level at 3.



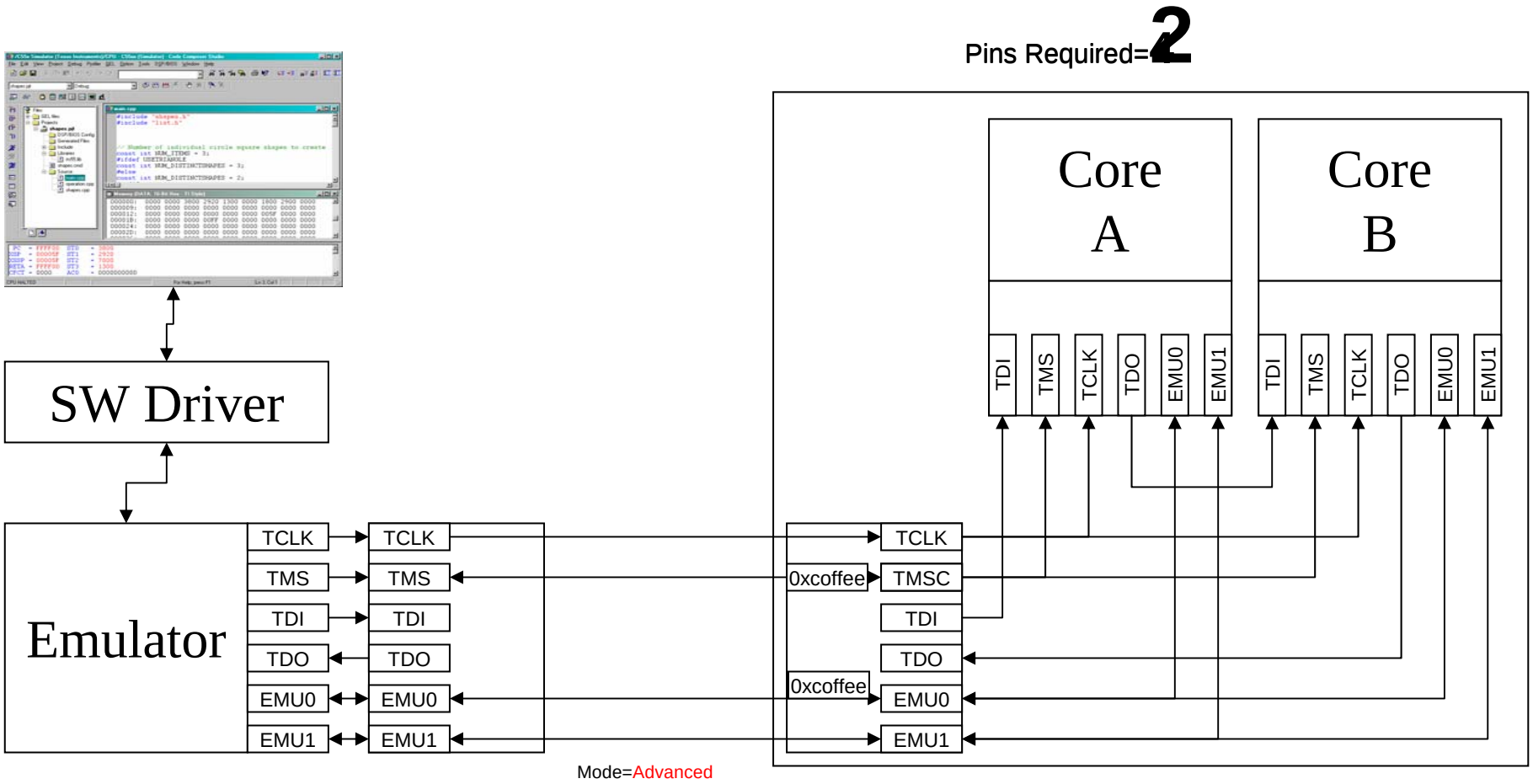
Key:

- Count the number of Zero-Bit-Scans (ZBS) to change the definition of BYPASS instruction.
- Lock control level when the Shift-DR state is reached.

Creating a Control Level

- Example: Steps to create a control level 3
  1. IR-Scan with BYPASS instr. — **BYPASS instruction**
  2. ZBS — **Increment control level from 0 to 1**
  3. ZBS — **Increment control level from 1 to 2**
  4. ZBS — **Increment control level from 2 to 3**
- Example: Steps to create a control level 5
  1. IR-Scan with BYPASS instr. — **BYPASS instruction**
  2. ZBS — **Increment control level from 0 to 1**
  3. ZBS — **Increment control level from 1 to 2**
  4. ZBS — **Increment control level from 2 to 3**
  5. ZBS — **Increment control level from 3 to 4**
  6. ZBS — **Increment control level from 4 to 5**

Extending 1149.1



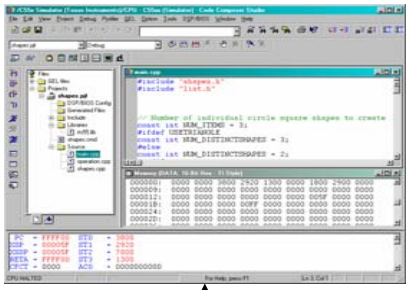
•EMU0 and EMU1 are typically used for to gather large amounts communication with a target application

•Using Background Data eXchange (BDX) and Custom Data eXchange (CDX), target information can be transferred.

•For maximum compatibility, CDX can be used to carry manufacturer defined protocols.

Extending 1149.1

Pins Required=**2**



SW Driver

Emulator

TCLK
TMSC
TDI
TDO
EMU0
EMU1

Core A

TDI
TMS
TCLK
TDO
EMU0
EMU1

Core B

TDI
TMS
TCLK
TDO
EMU0
EMU1

TCLK
TMSC
TDI
TDO
EMU0
EMU1

Mode=Advanced

How is it deployed?

P1149.7 Deployment Method

Capability classes:

3 classes - 4-pin using IEEE 1149.1 protocol

2 classes - 2/4-pin using IEEE 1149.1 protocol

P1149.7 “Classes”

Deliver:

a) 1149.1 extensions with standard protocol
b) 2-pin operation with advanced protocol
c) Bi-modal operation with plug and play

With five classes of capability:

- Class **T0** – IEEE Compliance for chips with multiple TAPs
- Class **T1** – Add control functions/preserving IP (e.g. chip reset(s))
- Class **T2** – Add chip selection for series and star configurations
- Class **T3** – Add two pin operation
- Class **T4** – Add instruction/custom pin use to two pin operation

IEEE P1149.7 Class Details

Class **T0**	• Ensure compliance with 1149.1 to enhance compatibility with industry test infrastructure	• After Test-Logic-Reset (TLR) multi-TAP devices: •Conform to mandatory 1149.1 instruction behavior •1-bit DR-Scan for bypass instruction • Addresses stacked die and multi-chip module needs
Class **T1**	• Power: Test logic power-down	• 4 Power Down modes friendly to: Board Test, Chip Test, and Application Debug
Class **T2**	• Performance: •Shortened multi-chip scan chains •Glue-less star configuration	• Chip Level Bypass • Built-in Chip Select Mechanism
Class **T3**	• Pins: Less pin and more functions •Faster downloads to target •Equivalent performance with fewer pins	• 2 pins provide scan, Test-Logic-Reset (TLR), and instrumentation (serialized transactions) • Download specific modes (Target Input only) • 2x Clock rate and optimized transactions
Class **T4**	• Instrumentation • Customization	• Concurrent Debug and Instrumentation using same pins • Instrumentation of data passed during Run-Test-Idle, Pause-DR, and Pause-IR states • Custom technologies can use the test access port pins in Shift-DR state. (ex: SWD, BDM, etc.)

Higher numbered classes operate with lower numbered classes

How will P1149.7 be used?

- **Class T0/T1 – any system, mix/match with 1149.1**
- **Class T2**
  - **Series topology -** Mix/match with 1149.1 devices
  - **Star topology -** Match with 1149.7 Class 2
- **Class T3/T4 – (4-pin)**
  - **Series topology -** Mix/match with 1149.1, T0, T1, and T2 devices
  - **Series topology -** Mix/match with T3/T4 devices, operate as 2-pin
  - **Star topology** – Mix/match with T2 supporting Star, T3/T4
- **Class T3/T4 – (2-pin) –** Mix/match with T3/T4 devices**:**

1149.1 and 2-pin T3/T4 devices may share either TCK or TMSC but not both if they are used together. The 2-pin and 4-pin interfaces may be also be kept separate.

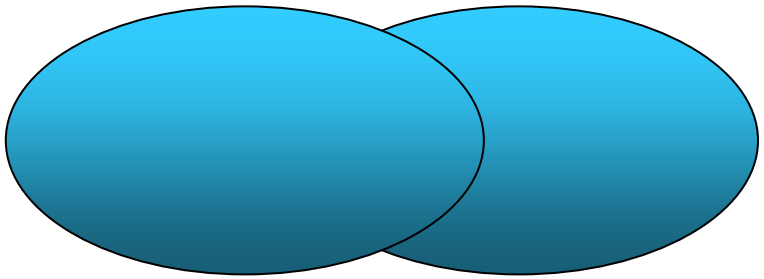
Projected adoption profile

- **Class 0:**
  - Should be no barriers
- **Class 1:**
  - Systems with embedded cores/application dev. needs
  - Some FPGAs
- **Class 2 :**
  - Systems with large number of chips
  - Systems with embedded cores/application dev. needs
- **Class T3/T4 – (4-pin) :**
  - Mass market devices that may be mixed with T3/T4 chips in system
  - Systems with applications development needs
- **Class T3/T4 – (2-pin):**
  - Wireless handheld devices
  - Consumer products

Where does P1149.7 take us?

Here are the choices >>

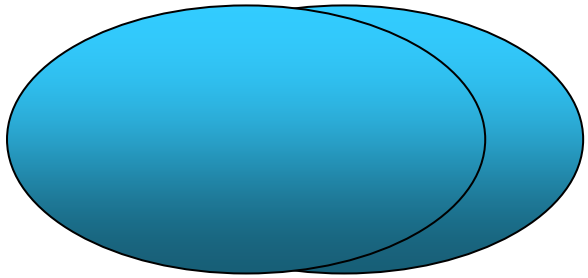
1149.1 Test and Debug Overlap



Test – easier

Debug - harder

1149.7 Test and Debug Overlap



Test – a bit slower

Debug - easier