Processor-Controlled Test Enhances EMC’s Test Effectiveness

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Types of Board Test

• **Intrusive Board Test (IBT)**
  - Requires test pads on every net, 1000’s of connections
  - Physically probes the board with spring loaded probes
  - ICT (In-Circuit Test on bed-of-nails)
  - MDA (Manufacturing Defects Analyzer on bed-of-nails)
  - FPT (Flying Probe Test on custom fixture)

• **Non-Intrusive Board Test (NBT)**
  - Also known as Embedded Test
  - Requires relatively few wires hooked to UUT
  - Boundary Scan Test
  - Processor Controlled Test (PCT) or Processor Emulation Test
  - Interconnect Built-In Self Test (IBIST)
  - Instruments or Internal JTAG embedded in chips (IJTAG)
  - Embedded Power Rails Test (On-Board Measurement of Voltage Rails)

• **Custom Functional Test (CFT)**
  - Custom written board functional “diagnostic” tests
  - Custom written system functional “exerciser” tests
What is Processor Controlled Test (PCT)?

• Also known as Processor Emulation Test
• Others call it “JTAG Debugger”, “Micro-Master”, “eJTAG”
• Processor Emulation or In-Circuit Emulation (ICE)
  – Software developer oriented (Engineering)
  – Uses XDP debug port on processors to gain access
  – Uses high-level, assembly language, and micro-code
  – Difficult for CMs and Debug Techs to use
• Processor Controlled Test (PCT)
  – More Manufacturing oriented
  – Uses XDP debug port on processors to gain access
  – Controls the CPU and all chips / buses on the UUT
  – Runs test programs on CPU without BIOS or Memory working
  – Loads small, targeted tests in instruction cache or RAM and executes them
• Advantages of PCT
  – Uses pre-programmed library of CPU and Chipset models
  – Easier and faster to write tests
  – Simple Command line interface for Techs
  – Faster than CFT and requires less resources
  – Only easy way to debug a board that won’t boot
How does PCT work?

- PC Software controls CPU through PCT POD & Adapter
- Puts CPU into debug mode using reset and writing CPU registers
- CPU registers in turn initialize and operate busses at normal speeds
- Tests progress outward from CPU one chip at a time until all chips are tested
- No need for DRAM, or BIOS, or Flash memory to be working or loaded
- Libraries of chip models make init and operations easy to program
PCT Test Philosophy

- Unit Under Test (UUT) powered up in fixture or product chassis
- Emphasis on Hardware debug and in-line testing in MFG
  - Can run tests even when board will not boot
- PC based emulator can connect directly to CPU in UUT via dedicated (XDP) interface using ribbon cable (Min 12 wires needed)
- Tests structured to Configure/Test each device moving out from CPU
  - Begin at basic level with Boundary Scan check on CPU pin levels
  - Check some CPU internal registers
  - Configure/Check memory controller
  - Initialize/Check DIMM memory
  - Configure/Check I/O controller
  - Continue to configure/check all hardware right out to and including testing of connectors on I/O cards
  - Check functionality of all major interfaces including; FSB, QPI, PCIe, FBD, SPI, I2C, etc
PCT Emulator Hardware
Why Has EMC Adopted NBT?

- **Problems with Intrusive Board Test (IBT)**
  - IBT includes ICT, MDA, FPT
  - Losing test pads (and coverage) on every new design due to high speed buses
  - Probe fixtures expensive and impractical during proto stage
  - Probe fixtures time consuming and difficult to change for ECOs
  - IBT cannot test for boot-up ability or test ICs functionally
  - IBT cannot test components or buses at native speeds
  - Tester time is expensive, so cannot program large flash memory

- **Issues with Custom Functional Test (CFT)**
  - Does not provide adequate fault isolation (<20%)
  - Often not available during proto stages (6-8 weeks after first hardware)
  - MFG depends heavily on Software Engineering for changes to CFT
  - CFT cannot be used if board won’t boot (Most common cause of pre-ESS failures)
  - Difficult to support and train CMs in Far East
  - Cannot debug non-seated DIMMs, bad flash memories, bad BIOS prom, etc.
  - Needs long test times due to overlap and re-booting (>60 minutes)
  - Long time to download CFT into product flash memory
Why Adopt NBT & PCT?

- Addresses most problems with IBT and CFT
- Shorter Development time vs. CFT (2 weeks vs. >8 weeks)
  - Early prototypes can have functional test & flash programming
- Faster overall test times (10 minutes vs. >60 minutes)
  - Lower Capital Equipment costs due to fewer testers needed
- Much better debug times with GUI (1 hour vs. >5 hours)
  - Lower costs at CM & less skilled debug techs
- No need to download a huge program to get functional test
- Only practical method to debug boards that do not boot-up
- Faster eeprom / flash programming than ICT
- Can diagnose any DRAM or FLASH / BIOS memory problems
- No need to store programs in BIOS, POST or FLASH mems
- CFT programmers reluctant to develop embedded tests
• Bscan, & IBIST
• Low Test Capital Cost
• Rapid Deployment
• Faster Issue Discovery
• PCT used for Debug only
Converged Basic Functional Test (BFT) Hardware Solution
BoundaryScan + PCT

• BFT converges BScan and functional PCT test capabilities
  – Uses same test station as BScan, so no added hardware cost or test stage
  – Needed to get better diagnosis software at the CM for functional test
  – Needed to save capital costs on BFT to compete with Functional Test hardware
  – Reached cost parity due to shorter test time (thus fewer testers) on PCT
  – Needed to diagnose “No-Boot” and Power problems to boost CFT and FC-MAT yield

• BScan / PCT merger facilitates cost savings over next few years
  – Combine BScan and PCT pods into 1 pod saves on Pod cost
  – Potential to use one software license to drive BScan & PCT could reduce license cost
  – PCT reduces debug repair costs & eases lack of ability to use scope probes

• New solution makes DFT easier by requiring less connectors on the product for BSCAN/IBIST/PCT Test
  – Makes for a simpler test setup and fewer cables
  – Supports our vision to have one test connector, make all test connections
  – Present products use a 28-pin connector to provide all test connections
Leverage emerging Intel IBIST and IC-BIST capabilities with standard Boundary Scan Interface

Utilize IC-BIST, Intel IBIST and PCT to verify EMC hw design

Working with IC component industry to develop ability to run internal instruments and BIST functions on the PC Board

Implement BFT in forward flow & reduce MFG dependency on CFT

Provide ultimate diagnosis tool to debug prototypes and DVT failures

Single test connector utilized company wide
  - Hardware Engineering, Software Engineering, MFG Engineering
  - MFG production, Failure Analysis Engineering

Added DC-DC Converter tests by using on-board sequencer MCU
Converged BFT Hardware Solution
In-Line Structural / Functional Test

- Bscan, IBIST, BIST, & Functional Test
- Low Test Capital Cost
- Extensive Capital Test Reuse
- Rapid Deployment w/ High Coverage
- Faster Issue Discovery
- Less Reliance on Custom Diags

**Faster TTM with Product Stability**

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<tr>
<th>Legend</th>
<th>Description</th>
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<tr>
<td></td>
<td>Structural Test @ CM (SPI = Solder Paste Inspection)</td>
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<tr>
<td></td>
<td>Structural Bscan Test @ CM</td>
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<td></td>
<td>Functional Test Custom Diag @ EMC</td>
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<td></td>
<td>(FC MAT = Final Config &amp; Maturity Test)</td>
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<td>Reconfig Assy Step (CTO = Config To Order)</td>
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Advantages of PCT in Production line

- Finds faults & trends early in production process
- Finds faults & trends faster than CFT in production process
- Changes in BIOS or POST have no effect on PCT tests
- No waiting for BIOS/POST updates to run tests
- Support comes entirely from MFG Engineering
- Easy to make updates/changes to test programs
- Easy to script and hook to data collection systems
- More stressing of boards/components than bios or POST
- Easier diagnosing to the chip or pin than functional tests
- Easy diagnosis of power up problems
Converged BFT Hardware Solution
In-Line Structural / Functional Test

- Bscan, BIST, & Functional
- Low Test Capital Cost
- Extensive Capital Test Reuse
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Real opportunity is to converge on a single platform, to allow us to develop and deploy comprehensive structural & functional test during DVT, and prepare for the embedded test opportunity that is coming, and reduce our reliance on custom diagnostics.
Advantages of BFT in Proto Stages

- Now launching BFT 2 weeks after 1st hardware arrives
  - CFT only available @ 6-8 weeks depending on platform
- Initial Tester in use @ 4 weeks
- Initial Tester @ CM in 5-6 weeks for 2nd Proto run
- Gets known good boards to developers faster

- Lack of scope access = techs can’t probe boards easily
  - They need a software debug tool more than ever
  - Reluctant at first “I don’t need a program to tell me what I already know”
  - Now say “I need any help I can get – this thing is my best tool”
  - Can’t use protocol analyzers & logic analyzers in debug due to time & cost constraints

- New high speed buses require prohibitively expensive test equipment
  - Embedded tests like IBIST can enable high speed serial testing in PCT
  - Developing internal IC instrument / Eye tests

- Program BIOS and POST early on – can debug when BIOS is broken
BFT Analog / Embedded Loopback Capabilities

- All CPU & I/O boards have power sequencer MCU
- Single test connector provides TWI connection to sequencer
- Sequencer monitors & adjusts all DC-DC power circuits
- If a power-up fault occurs, sequencer stores values of supplies
- BFT software can read and report fault data
- Developing use of vendors’ internal HS serial loop back tests
- Requires some DFT in design and vendor supplied firmware.
- Connects through JTAG or TWI connection.
EMC PCT Test Features

- Tests controlled and Pass/Fail results displayed via customized “Block Diagram” GUI or standard Emulator GUI
  - Can loop tests for debug purposes
  - Can view test scripts to understand test – CFT tests hard to understand what is tested
  - Techs can use script language to flip bits, exercise buses, read back data, etc.
  - GUI written by Cork, Ireland Test Engineers using PCT vendor’s standard API

- Test Time
  - Total test time of UUT with 2 I/O cards is <10 minutes/unit

- Coverage
  - 51% coverage on robotic fault insertion vs 35-40% on CFT
  - 90% diagnostic accuracy vs ~70% on CFT
  - In actual run of boards, of 11 faults found by PCT, 10 were predicted correctly
  - Still studying “diagnosability” comparison

- Yields
  - BFT yield was 83.5% (Boards had no ICT tests yet)
  - Subsequent CFT test had 92.8% yield.
  - PCT test was improved to catch more faults, so final CFT yield would be 94.2%
BFT Converged Hardware Solution
Signals Needed for PCT Test

- TCK, TMS, TDI, TRST to Processor
- TDO from Processor
- Main board reset to MCU
- Reset from Processor
- 3 BPM signals from Processor (Break Point Monitor)
- VTT
- GNDs
- Most are 1.1V levels
- Need to keep round-trip-time short
- EMC BFT runs at 10 MHz TCK
- PCT can run up to 20MHz
Conclusions / Future Needs

- PCT is integral part of BFT test suite
- Improves test coverage
- Improves Diagnosability
- Decreases Time To Market for new products
- Enables use of less experienced techs at CMs
- Need standards in test connections and fewer pins on connector
- More studies needed to establish solid cost savings
- Need to develop multiple test sites on one tester like CFT
- New PCT pods will be linked over Ethernet to one tester
- Targeting eventual replacement of CFT stage.
- Also looking at reduced ICT test functions to save ICT tester time