SiP-TAP: JTAG implementation for SiP designs

Contents

- SiP and TAP, what’s the problem?
- The SiP-TAP solution
- SiP-TAP in practice
- Summary
SiP and TAP

Why do we need a TAP?
- The method for test access
- Widely used (Test/Debug/CTAG-AMS)
- Standardized (IEEE Std 1149.1)
- Only a few pins
- Supports Defect Oriented Test
- Highly suited for detecting assembly failures

But:
The 1149.1 TAP does not support design hierarchy....

The JTAG Standard (IEEE Std 1149.1)

Statements from the JTAG standard, relevant for SiP design:
- A JTAG device may have only one Test Access Port (TAP).
- A JTAG device must have a BYPASS register which is exactly one cell long.
- If a JTAG device has an ID register, this register must be 32 cells long.
- A TRST* pin activation shall reset all test logic to the ‘Test logic reset’ state.
SiP with JTAG

SiP-TAP: The solution

Contents

- SiP and TAP, what’s the problem?
- The SiP-TAP solution
- SiP-TAP in practice
- Summary
The Solution: dies with SiP-TAP

TRST issues (1)  TRST – non compliant SiP!
**EBTW'06** TRST issues (2)  POR Circuit on Substrate

Requires extra POR circuit on substrate (implementation?).

---

**EBTW'06** TRST solution: POR Circuit on ALL dies with SiP-TAP

Chilworth, Southampton, UK
Die with SiP-TAP

- Extra TDI (STDI)
- MUX on TDI inputs
- Modified TAP Controller
- Modified TRST (TRST/POR-I/O pin)
- Transparent path from TDI to TDO

Chip with SiP-TAP

- 4 Pin TAP
- TDI and STDI are connected in the package.
- TRST/POR-I/O does not have to be connected to a package pin.
SiP-TAP in practice

Contents

- SiP and TAP, what’s the problem?
- The SiP-TAP solution
- SiP-TAP in practice
- Summary

Standard behavior after reset

SiP

Die 1

Core Logic

SDI

TMS

TDI

TDO

Por

Die 2

Core Logic

SDI

TMS

TDI

TDO

Por

Die 3

Core Logic

SDI

TMS

TDI

TDO

Por

Die 4

Core Logic

SDI

TMS

TDI

TDO

Por

Die 5

Core Logic

SDI

TMS

TDI

TDO

Por

Die 6

Core Logic

SDI

TMS

TDI

TDO

Por
Scan/Debug

 POR and 1149.1

1149.1 Standard Circuit behavior

POR

Vdd

TRSTn

TRST internal reset

Functional reset

Functional internal reset
POR and SiP-TAP

SiP-TAP Circuit behavior

POR

Vdd

POR-inhibit

JTAG POR-out

Functional reset

TRST internal reset

Functional internal reset

POR-I/O

TRST internal reset

Functional internal reset

- Open drain out,
- TRSTn in
Contents

- Introduction
- The SiP-TAP solution
- SiP-TAP in practice
- Summary

Summary

RESULTS:

- For the customer the SiP is a 1149.1 compliant device.
- Supports third party and legacy dies.
- Transparent path from TDI to TDO

REQUIRED:

- Extra TDI PAD (STDI).
- TRST/POR-I/O.
- Power-On-Reset circuit required.
- SW